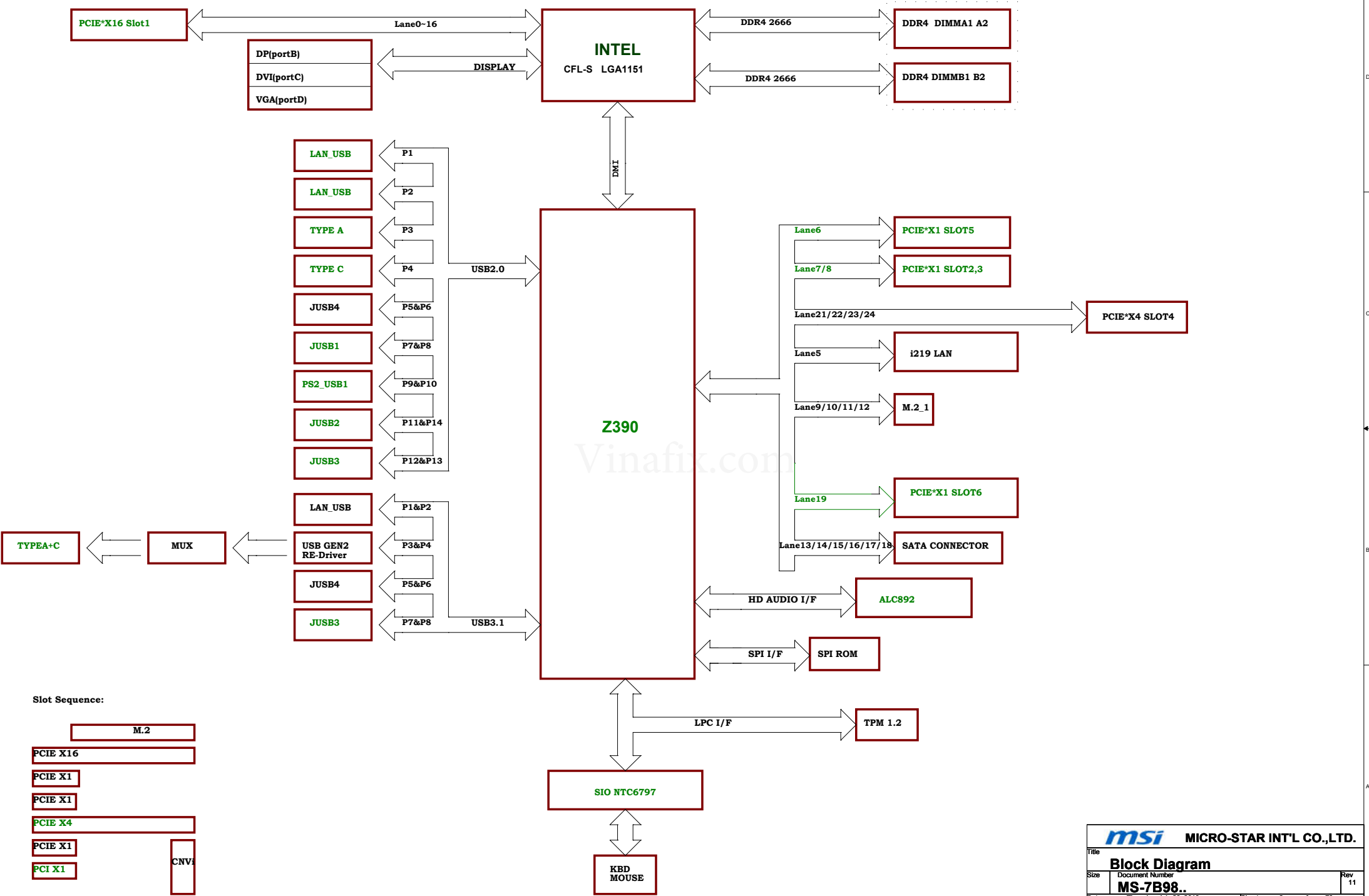
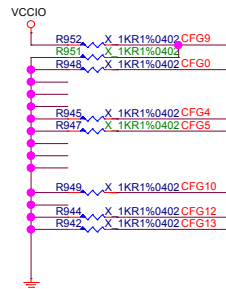
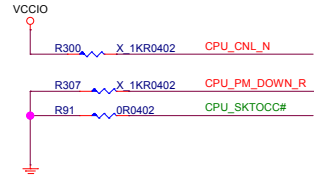
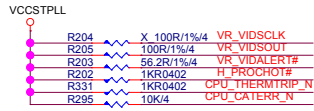


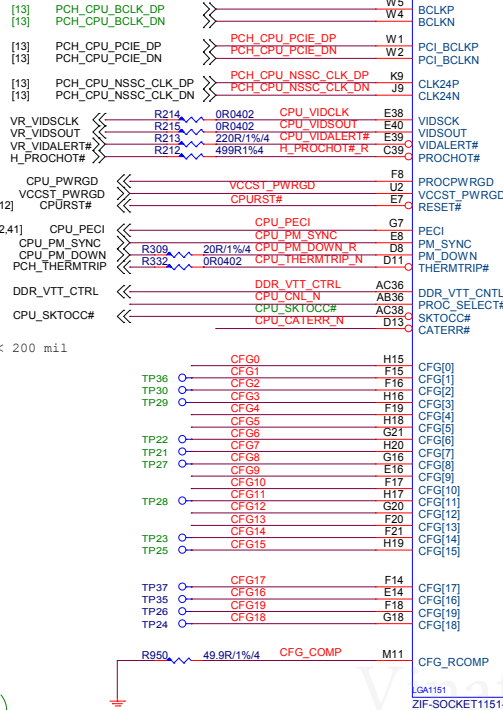
MS-7B98 Block Diagram



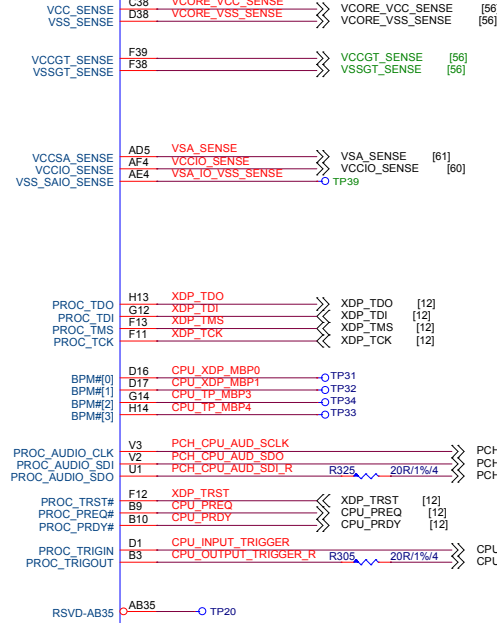


2017/7/13
Remove JP1 because JP1 combine to J1
Please see the D78 on page 54

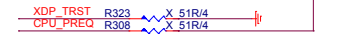
CPU_PM_DOWN_R < 200 mil



CPU1E CFL-S



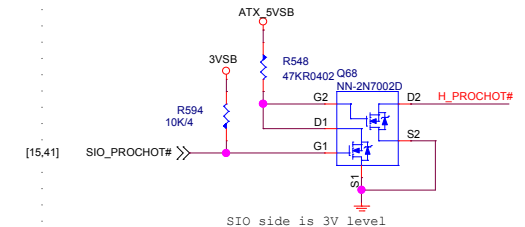
Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil



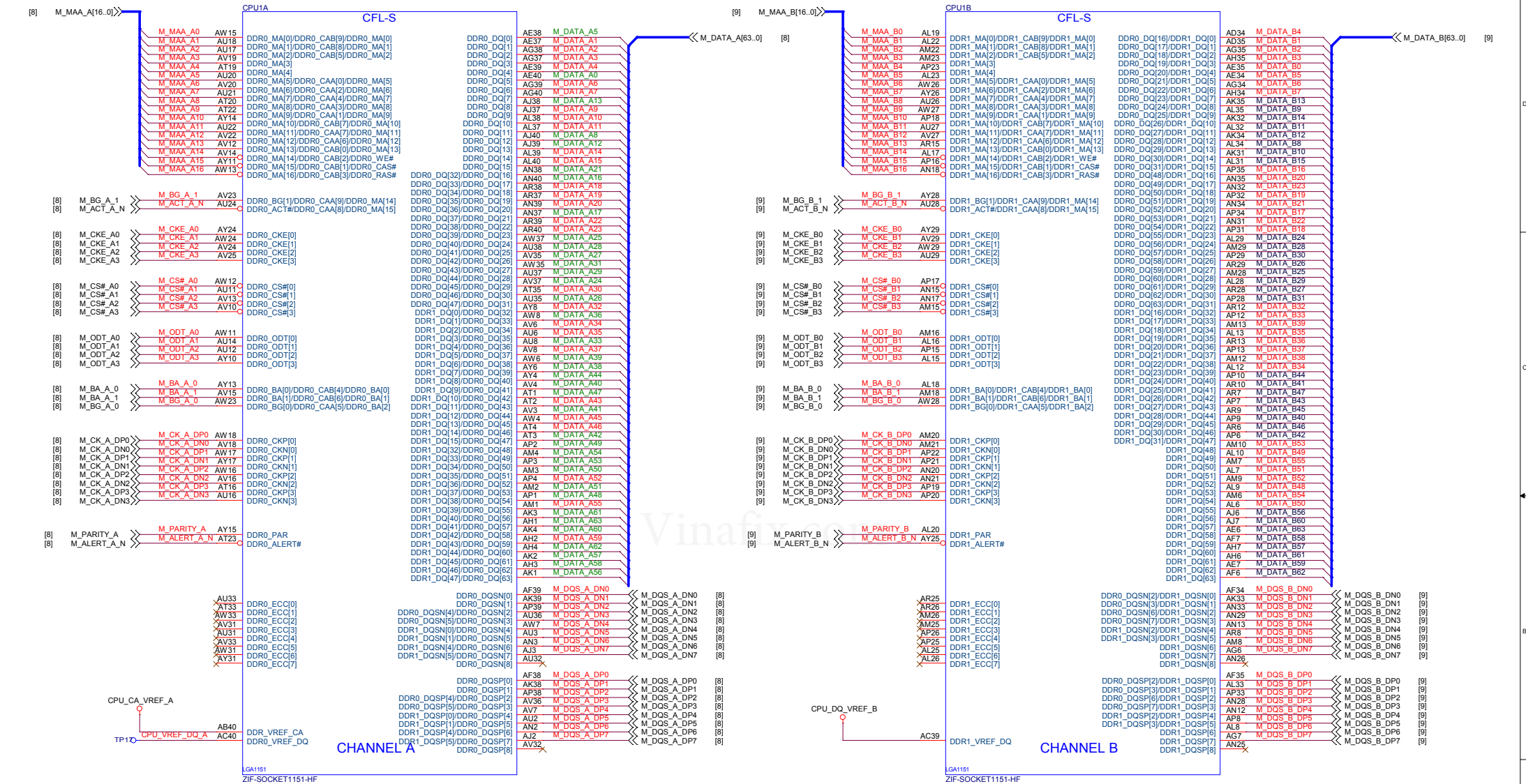
CFG Strap

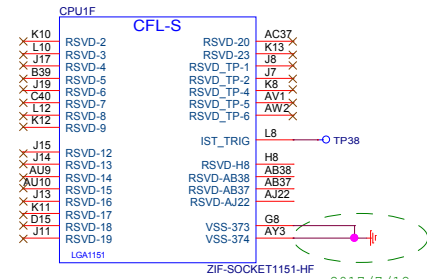
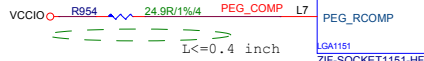
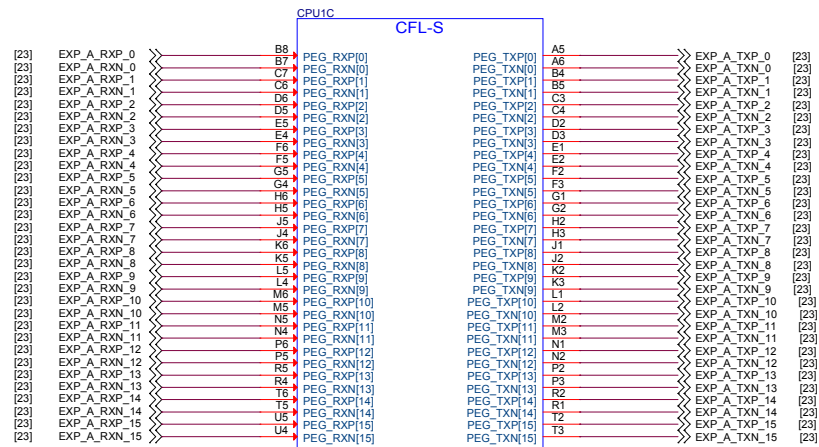
CFG Table

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEGCFGSEL[0]
6	DISABLE	ENABLE	PEGCFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD



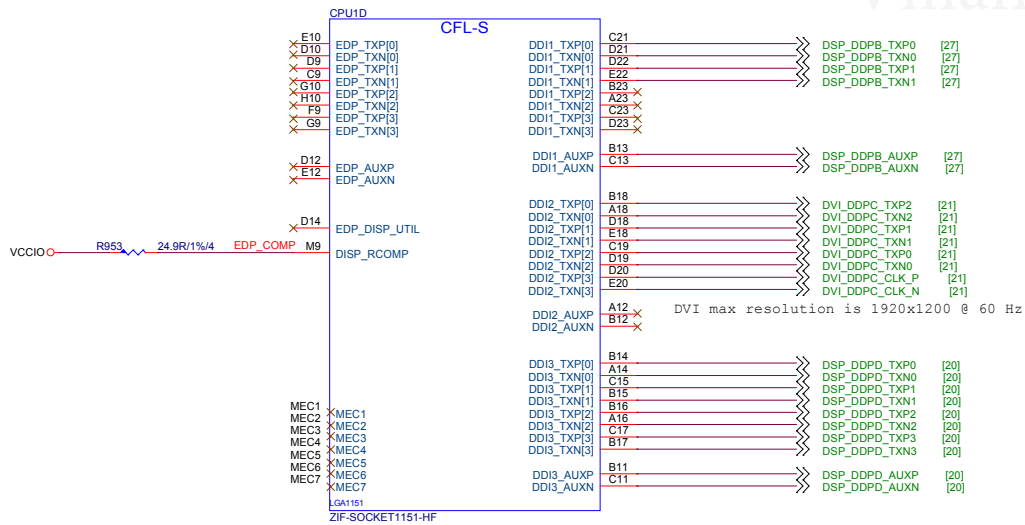
SIO side is 3V level

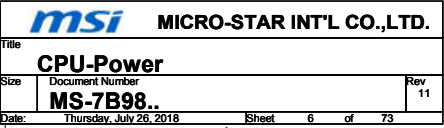


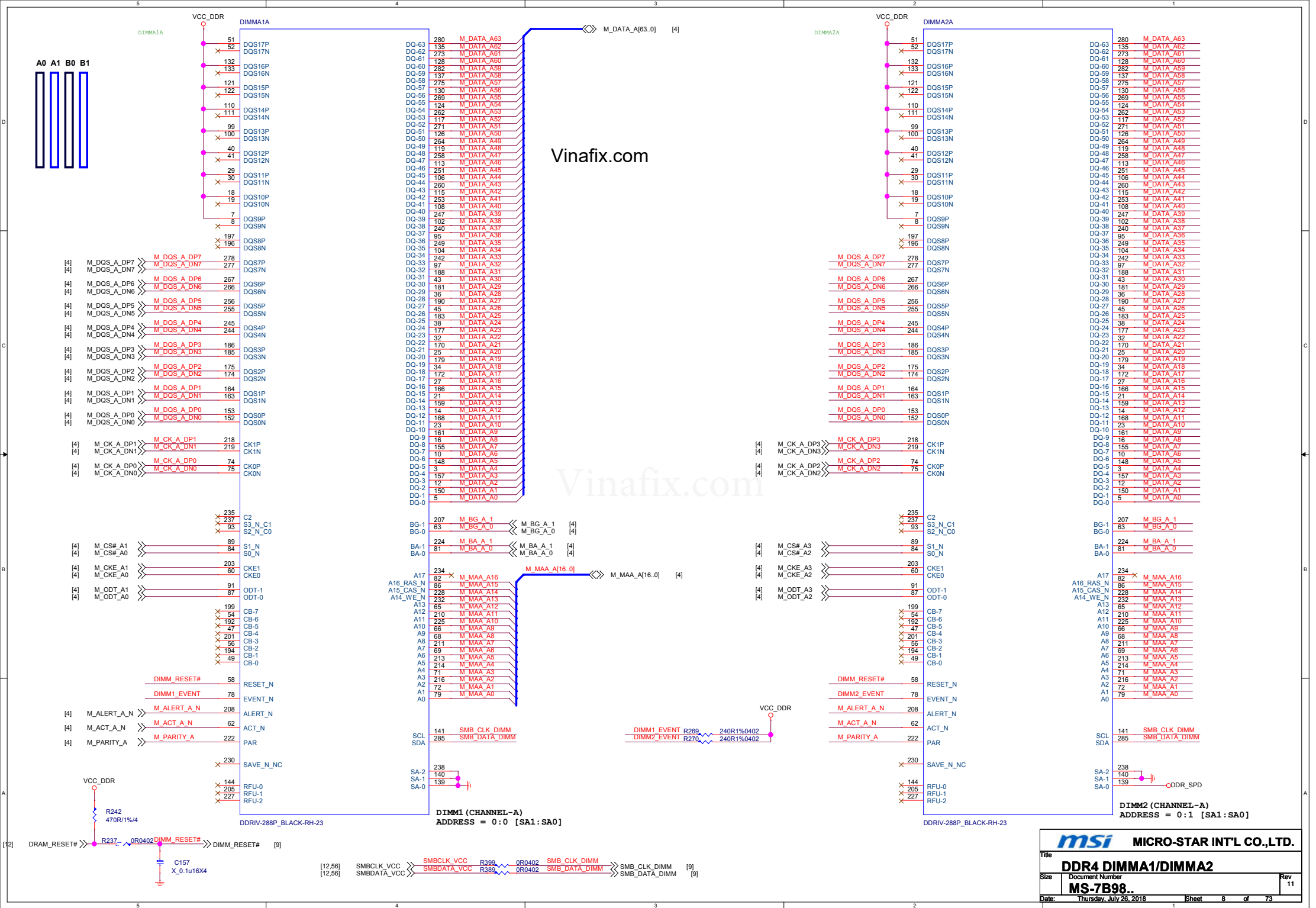


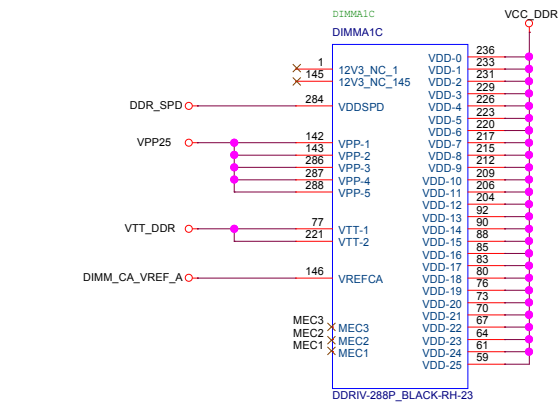
2017/7/12
G8 and AY3 can connect directly by CRB 1.0

Vinafix.com

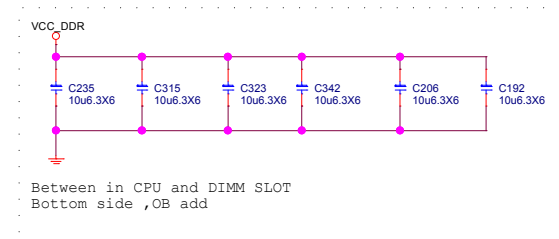
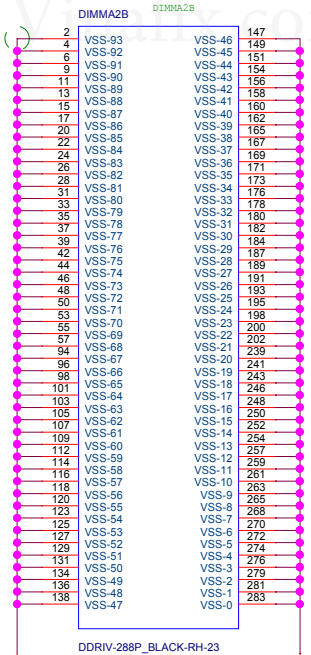
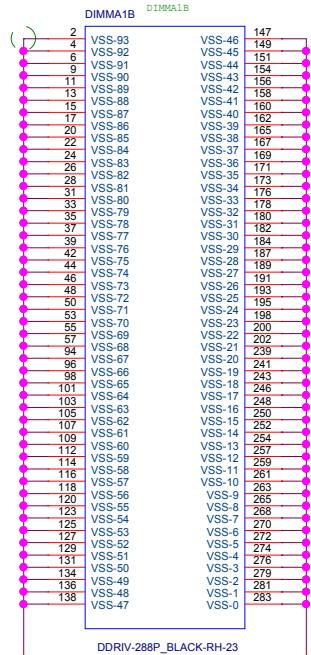
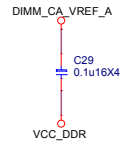
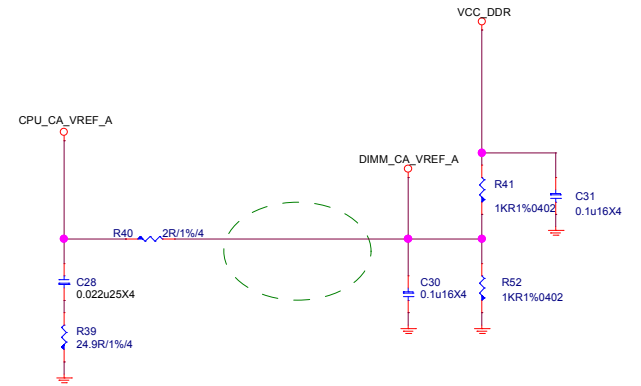
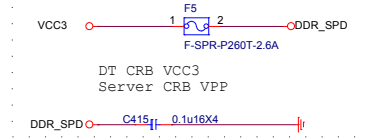
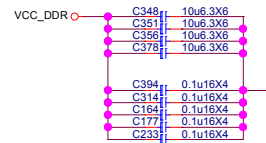
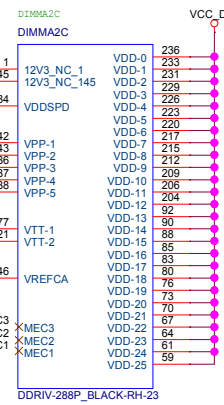
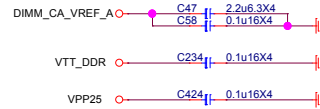
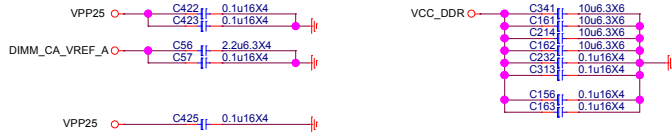
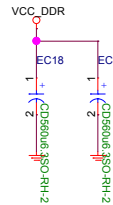




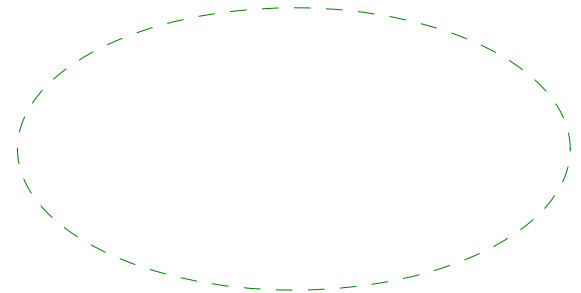
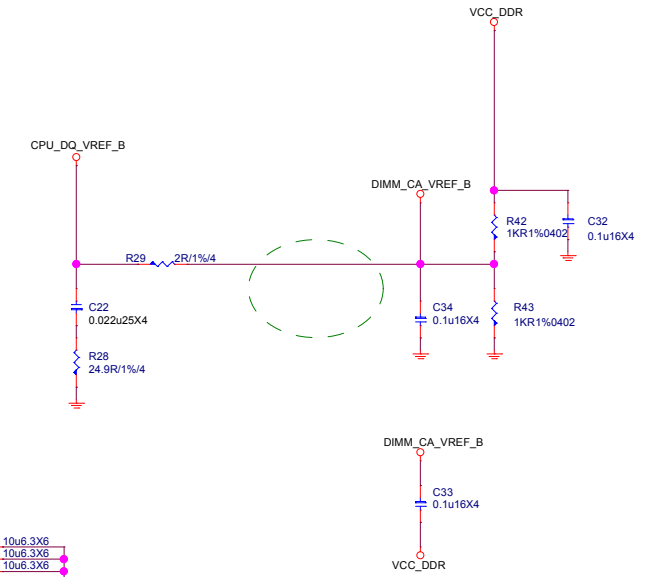
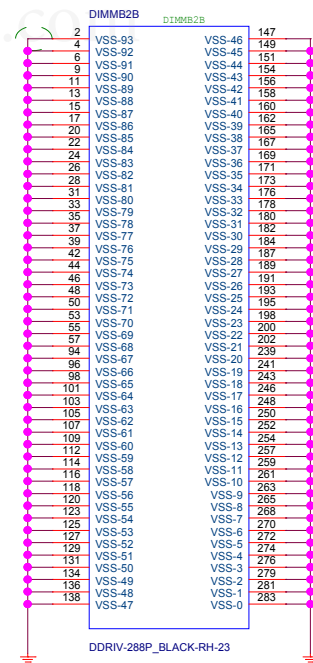
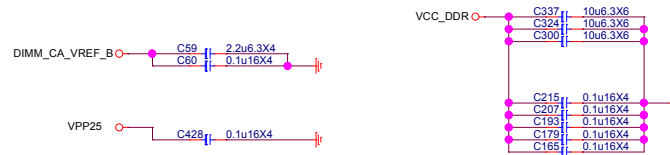
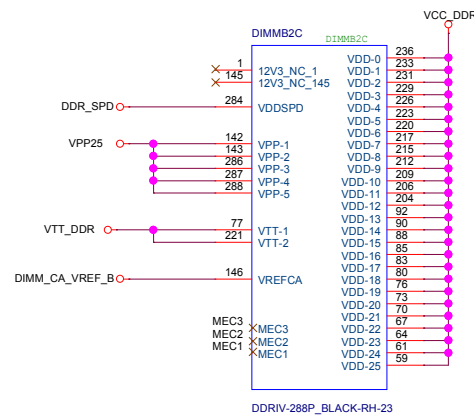
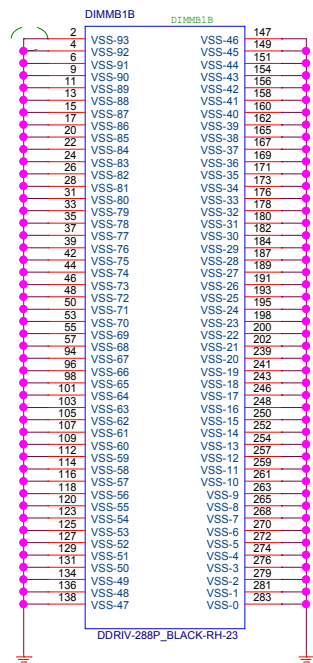
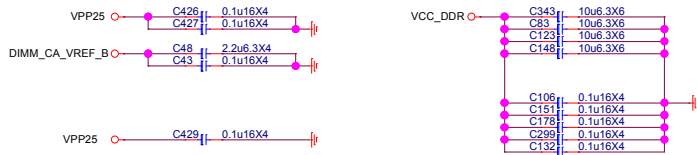
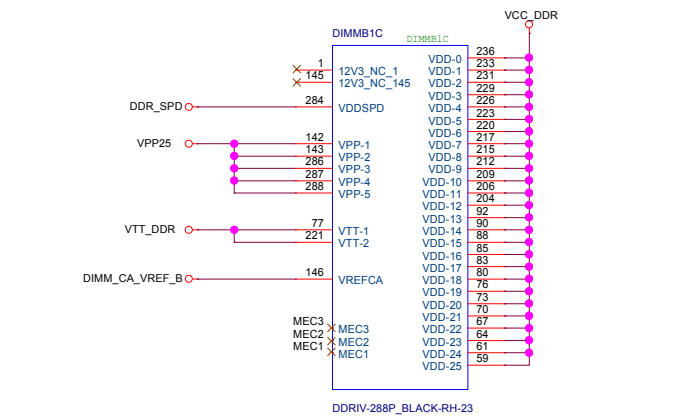


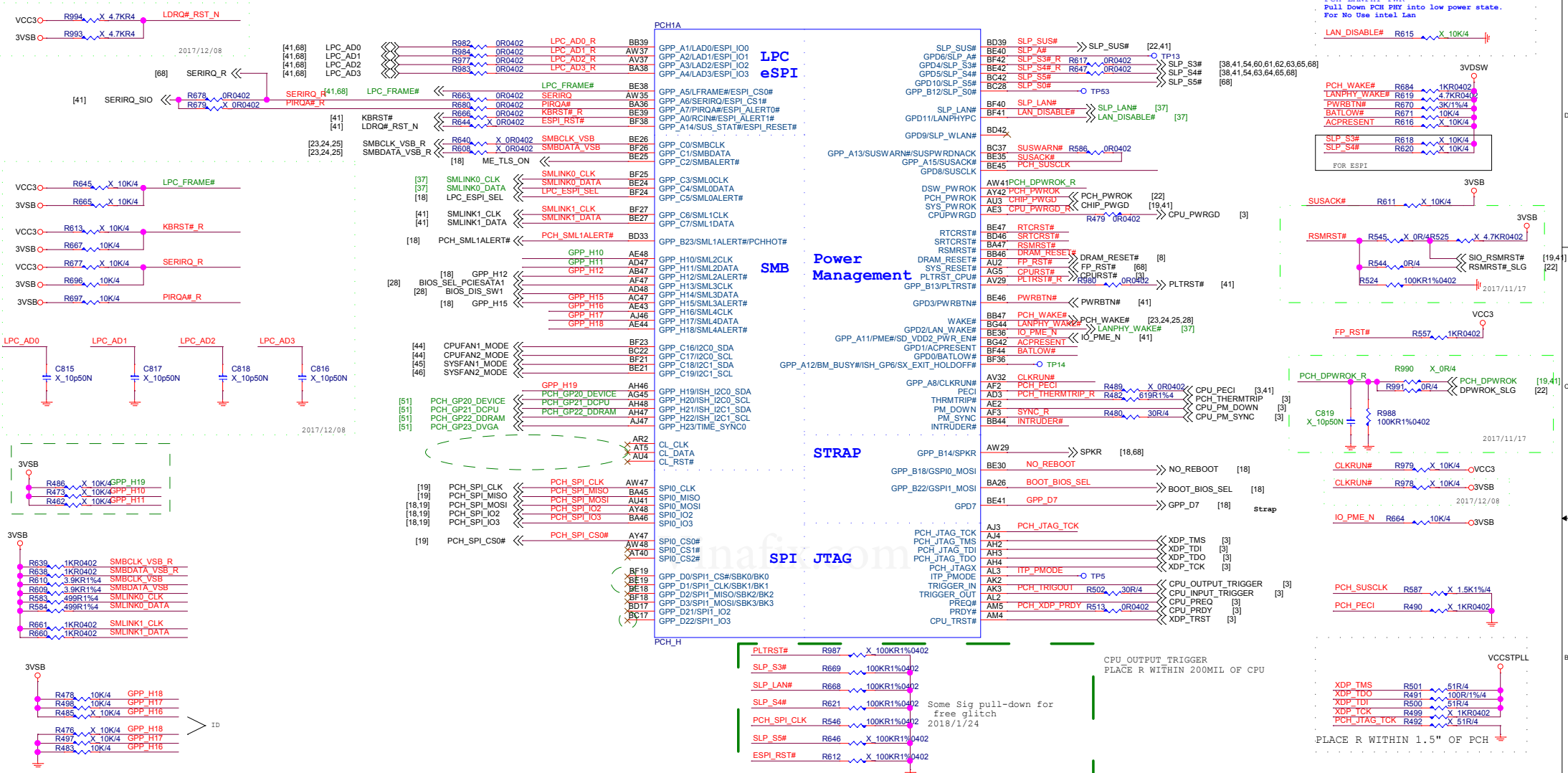


DIMM SLOT PN BY SPEC

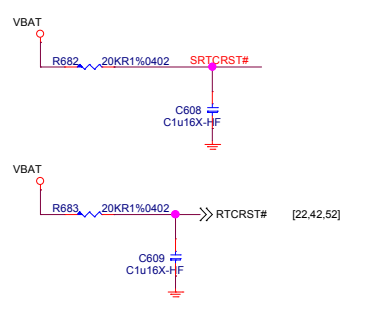


Between in CPU and DIMM SLOT
Bottom side ,OB add

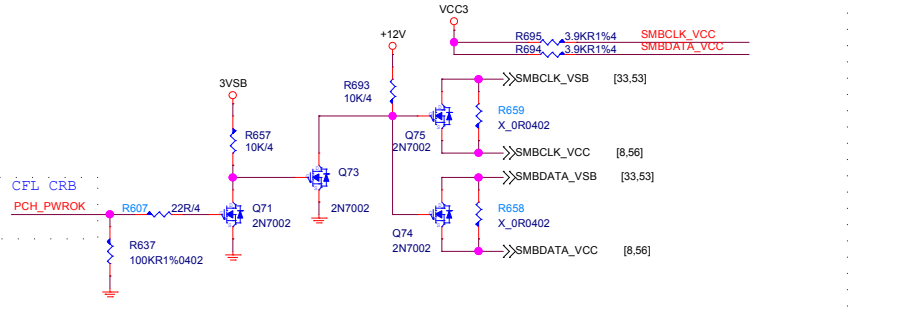
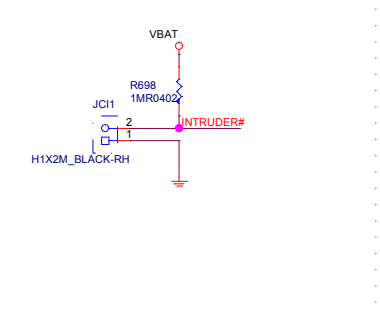


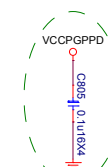
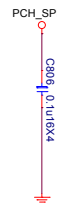
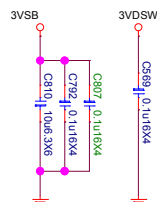
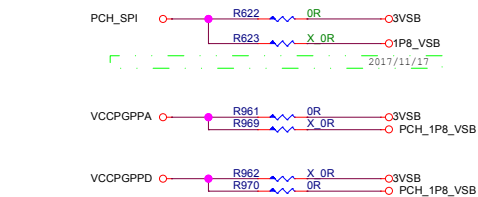
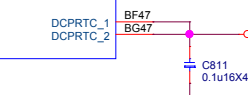
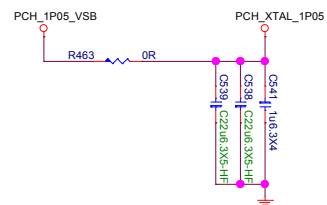


RTC



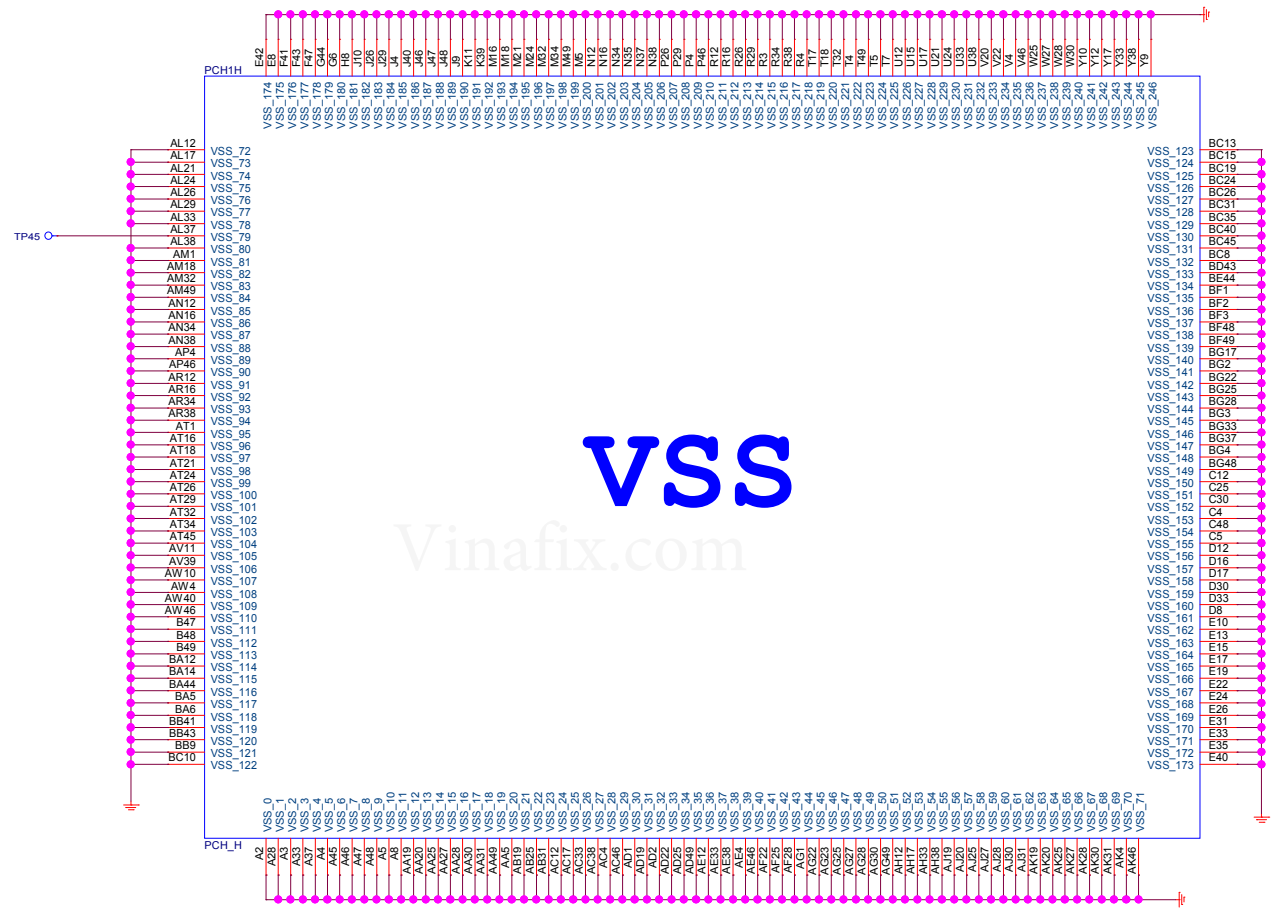
Chassis Intrusion



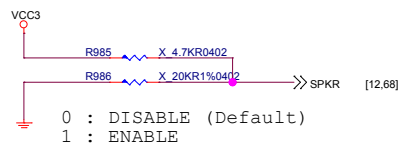


VSS

Vinafix.com

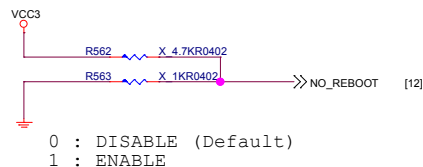


TOP Swap



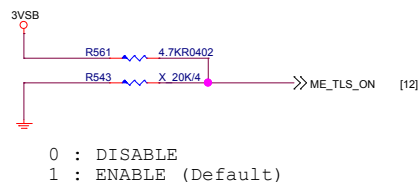
Internal pull-down is disabled after PCH_PWROK is high.

No Reboot



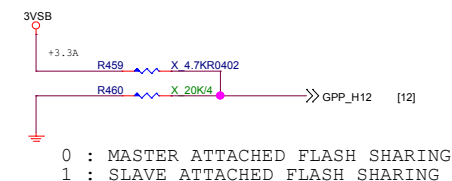
Internal pull-down is disabled after PCH_PWROK is high.

TLS confidentiality



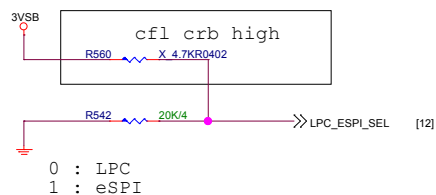
Internal pull-down is disabled after RSMRST# de-assert.

ESPI FLASH SHARING MODE



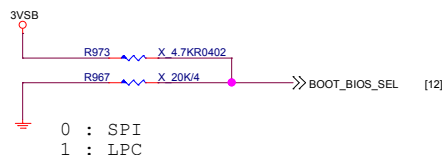
Internal pull-down is disabled after RSMRST# de-assert.

LPC eSPI Mode



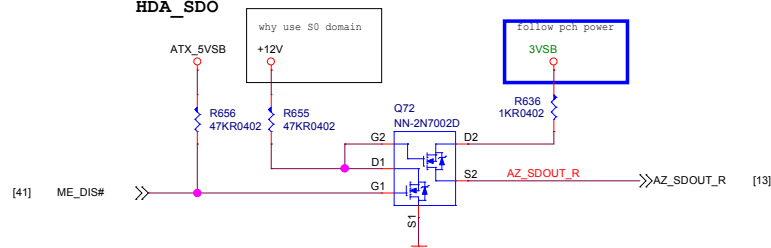
Internal pull-down is disabled after RSMRST# de-assert.

Boot BIOS



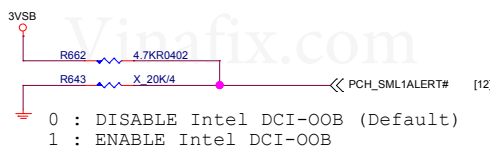
Internal pull-down is disabled after PCH_PWROK is high.

HDA_SDO



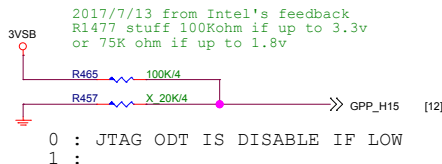
Internal pull-down is disabled after PCH_PWROK is high.

DCI ENABLE

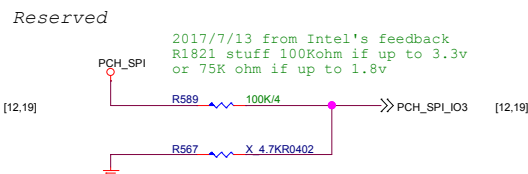
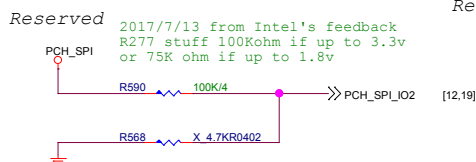


Internal pull-down is disabled after RSMRST# de-assert.

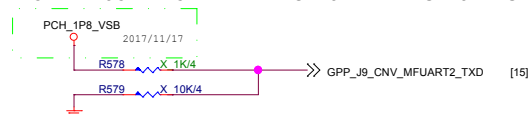
ODT DISABLE



Internal pull-down is disabled after RSMRST# de-assert.

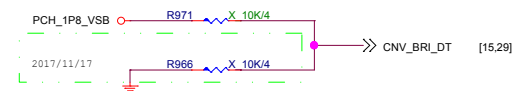


SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE



0 = VCCPSPI IS CONNECTED TO 3.3V RAIL (DEFAULT)
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

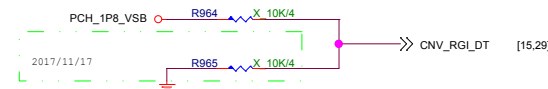
XTAL FREQUENCY SELECTION



1 = 24MHZ (25MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
0 = 38.4/19.2MHZ
XTAL_SEL1 :Internal Pull down

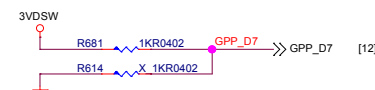
MODEM AND NFC REFERENCE CLOCK SOURCE SELECT

2017/7/12 from Intel's feedback
PU if the integrated CNV1 is enabled
PD if the integrated CNV1 is disabled



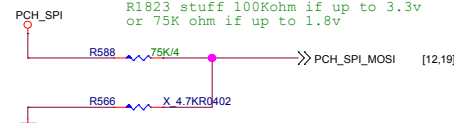
1 = CLKIN_XTAL_LCP
0 = XTAL_IN (CNP AND LCP SHARE XTAL)
XTAL_SEL2: Internal Pull High.

XTAL INPUT MODE



1 = XTAL INPUT IS DIFFERENTIAL
0 = XTAL INPUT IS SINGLE-ENDED
PCH HAS INTERNAL 20K PD

Reserved 2017/7/13 from Intel's feedback
R1823 stuff 100Kohm if up to 3.3v
or 75K ohm if up to 1.8v

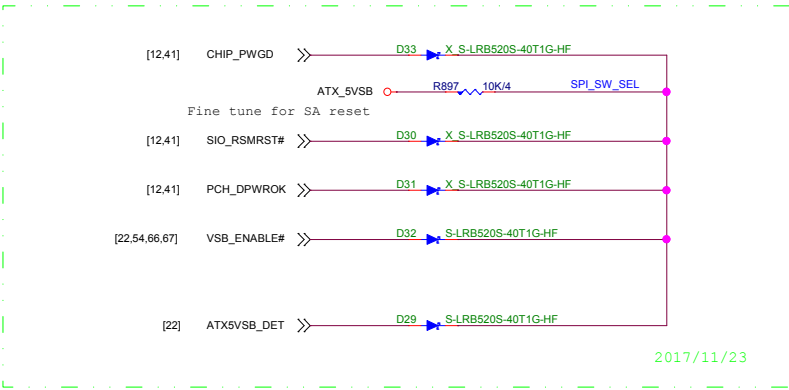
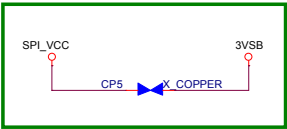
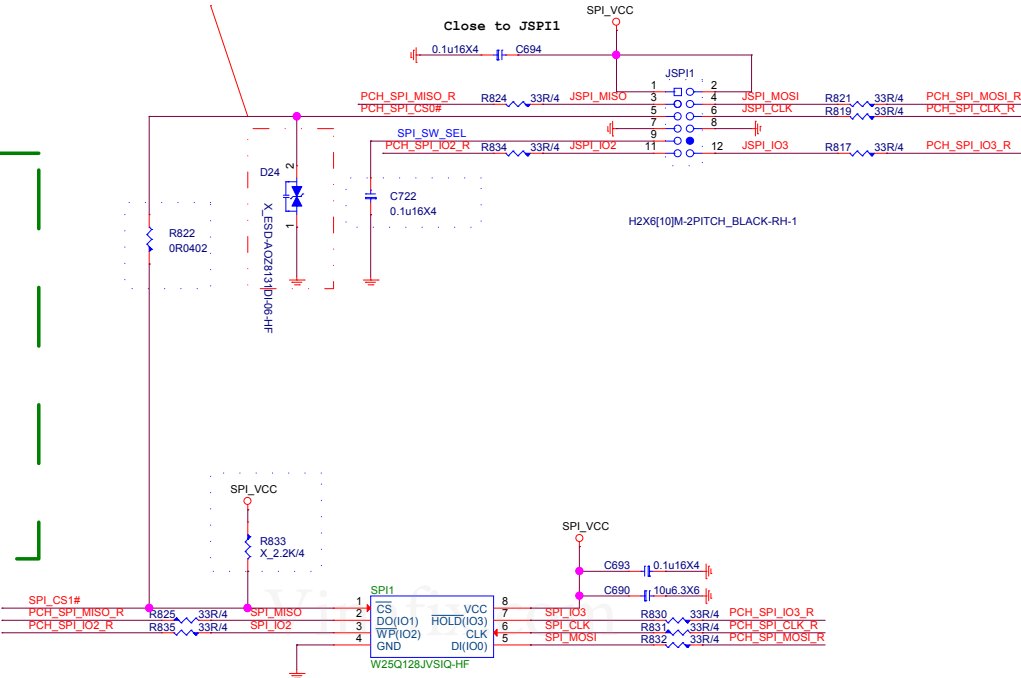


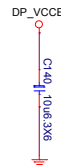
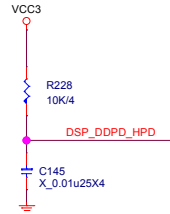
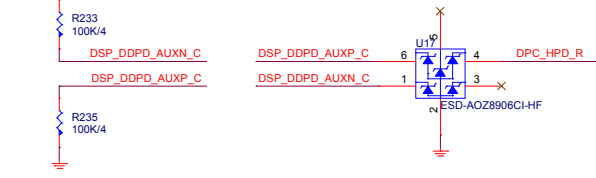
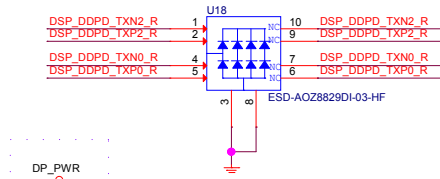
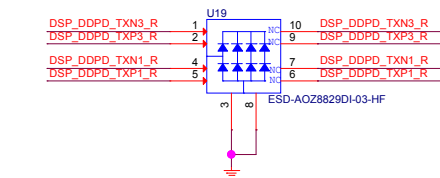
[12] PCH_SPI_CS0# << PCH_SPI_CS0#
[12,18] PCH_SPI_MOSI << PCH_SPI_MOSI R820 0R/4 PCH_SPI_MOSI_R
[12] PCH_SPI_MISO << PCH_SPI_MISO R823 0R/4 PCH_SPI_MISO_R
[12] PCH_SPI_CLK << PCH_SPI_CLK R818 0R/4 PCH_SPI_CLK_R
[12,18] PCH_SPI_IO2 << PCH_SPI_IO2 R826 0R/4 PCH_SPI_IO2_R
[12,18] PCH_SPI_IO3 << PCH_SPI_IO3 R816 0R/4 PCH_SPI_IO3_R

SPI CS# < 25pF
D0G-0402510-SI0

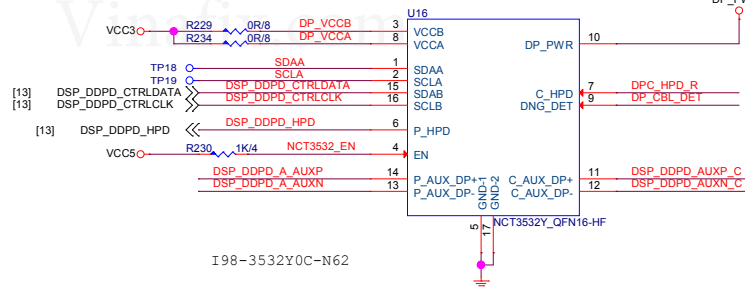
SPI_VCC
R827 X 1KR0402 PCH_SPI_IO2_R
Reverse Pull high @ PCH_SPIO2_R and PCH_SPI_IO3_R

PCH_SPI_IO3_R
R829 X 1KR0402
SPI_VCC

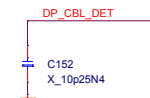
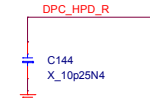
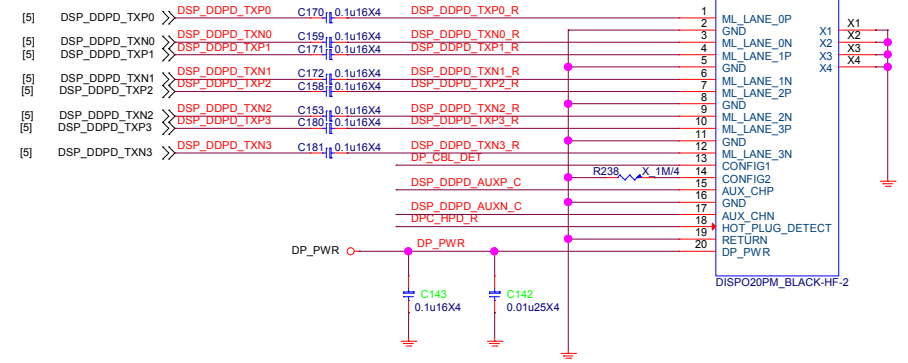




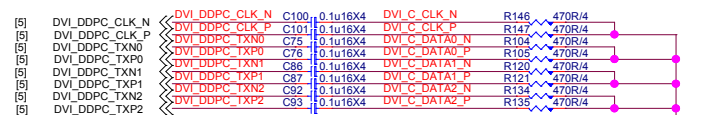
DP_VCCB trace don't less than 30 mil



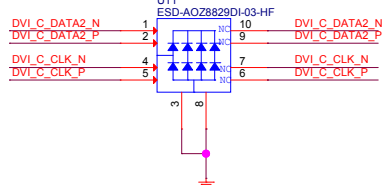
DP



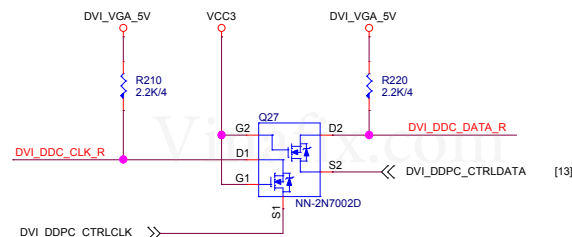
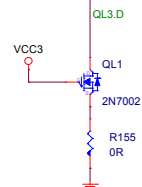
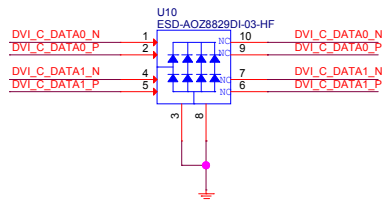
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



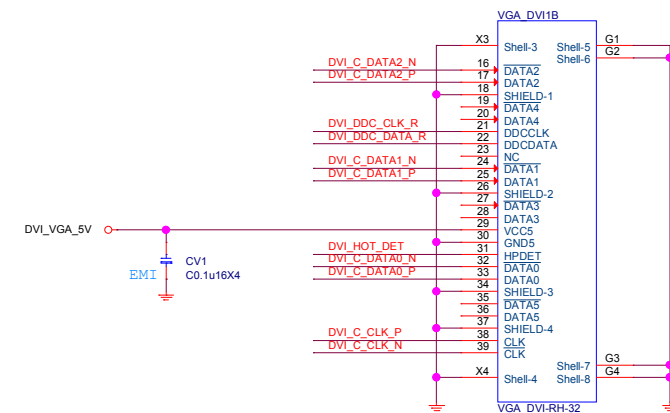
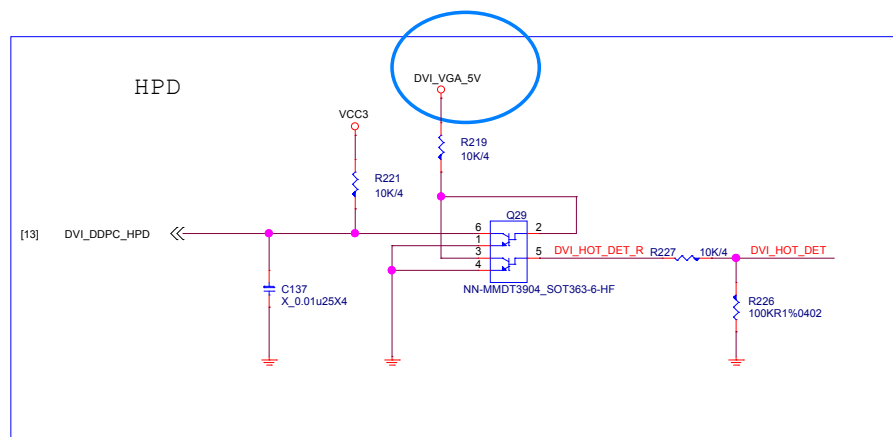
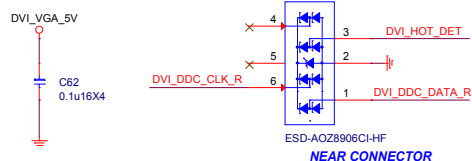
U26 AVL:D0G-05A050C-005
D0G-06A050C-A68



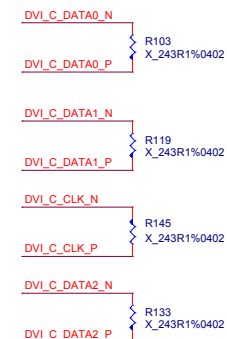
U27 AVL:D0G-05A050C-005
D0G-06A050C-A68



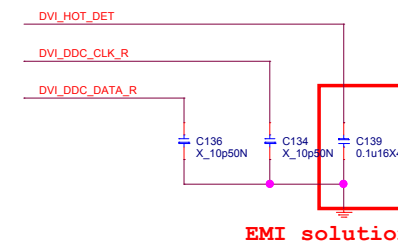
EMI Cap near connector DVI1



For EMI

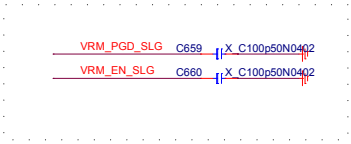
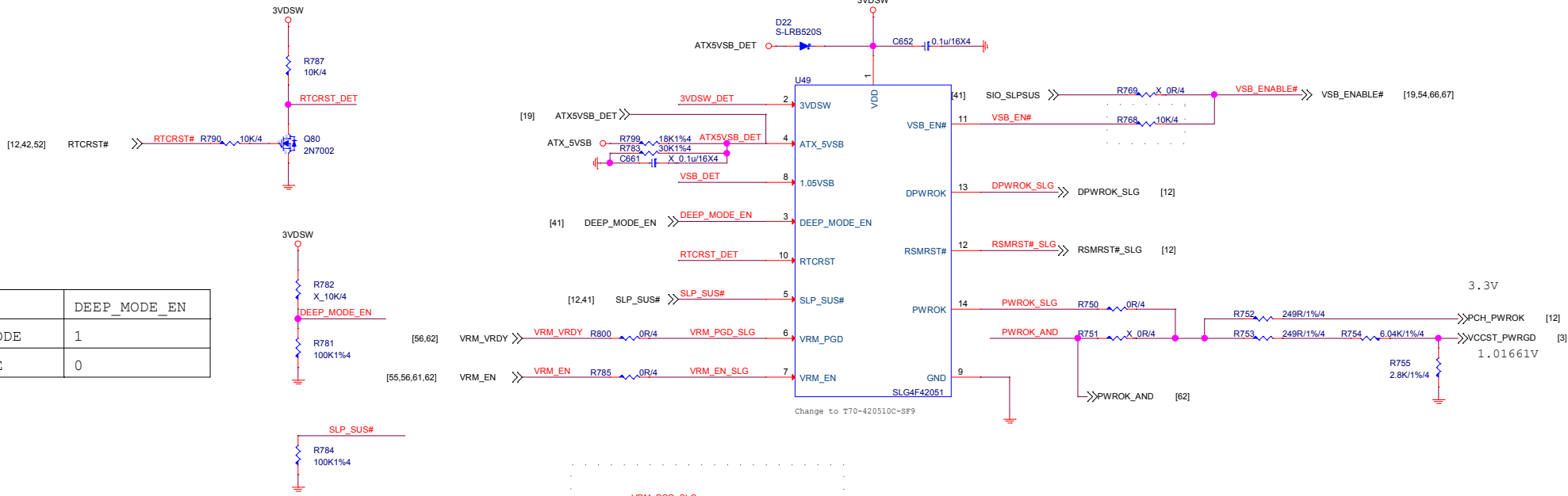


EMI

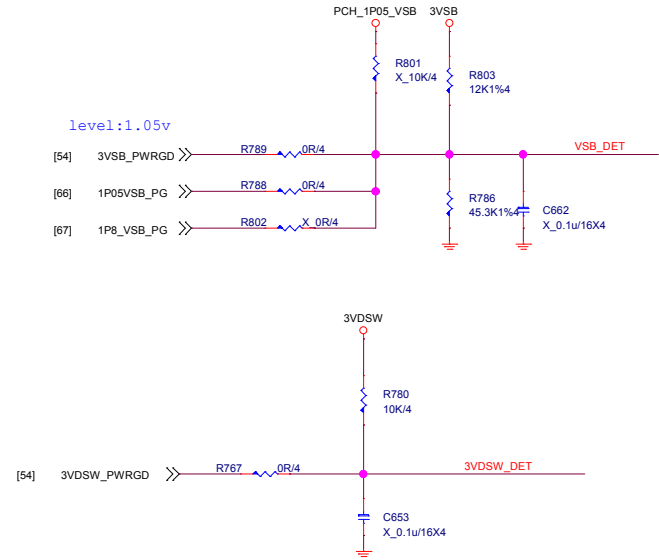


msi MICRO-STAR INT'L CO.,LTD.

	DEEP_MODE_EN
DEEP_MODE	1
S5_MODE	0



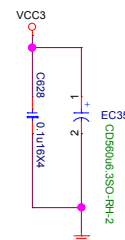
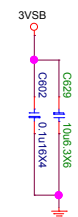
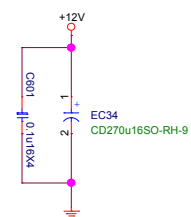
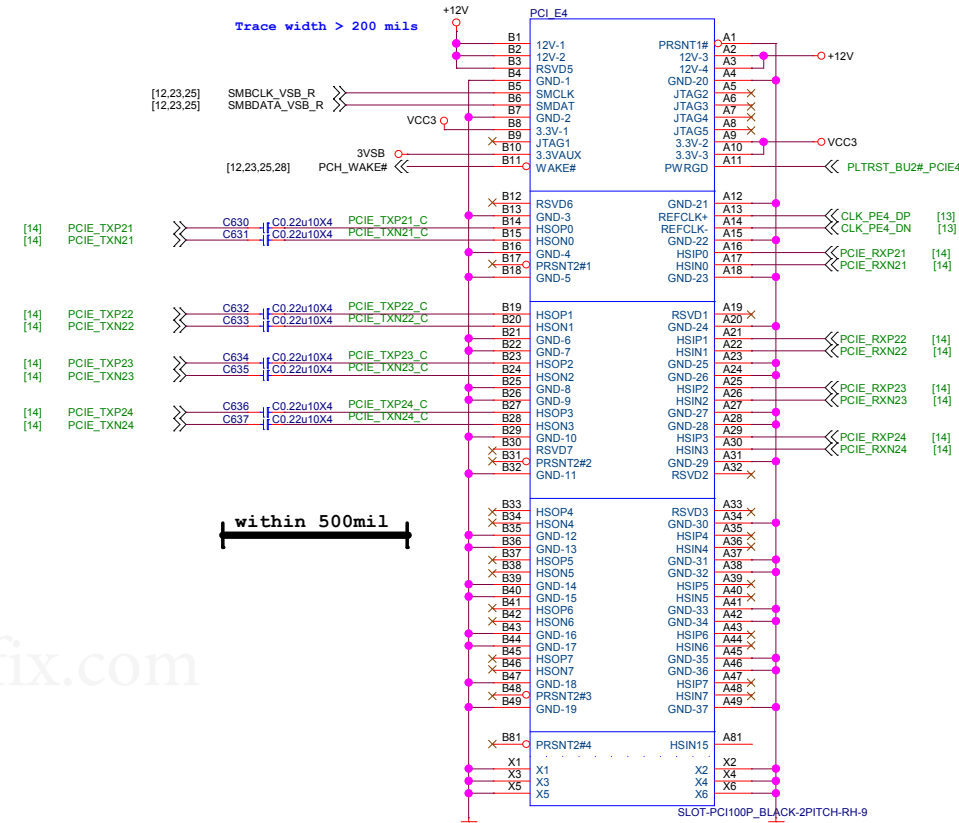
Vinafix.com



PCI Express X4 Slot

2.1A at +12V
3A at VCC3
375mA at 3VSB

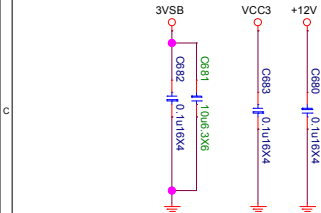
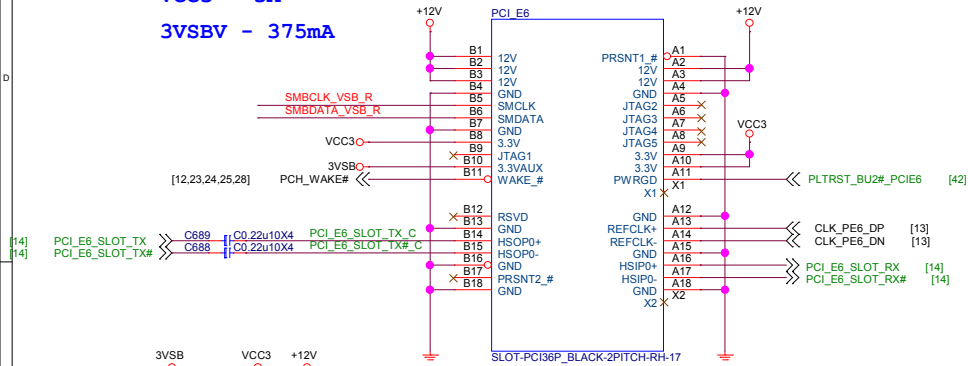
PCI_E4 share bandwidth with M2_2(M2_2優先)



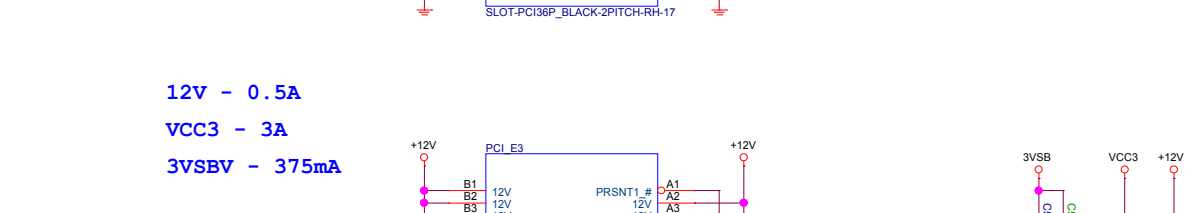
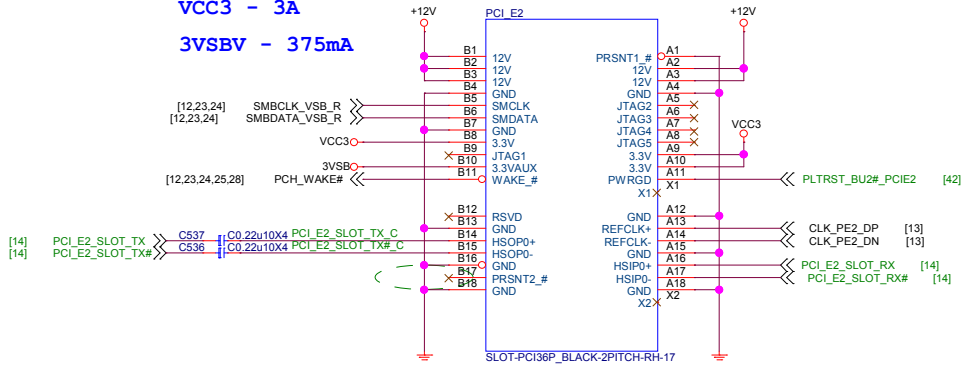
Vinafix.com

PCH PCIE X1 Slot

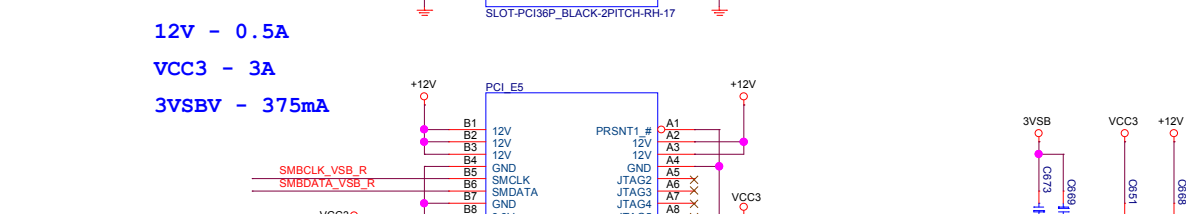
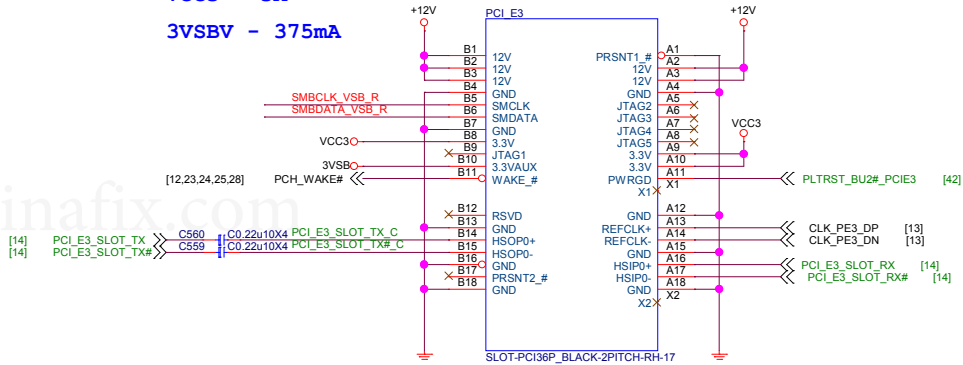
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



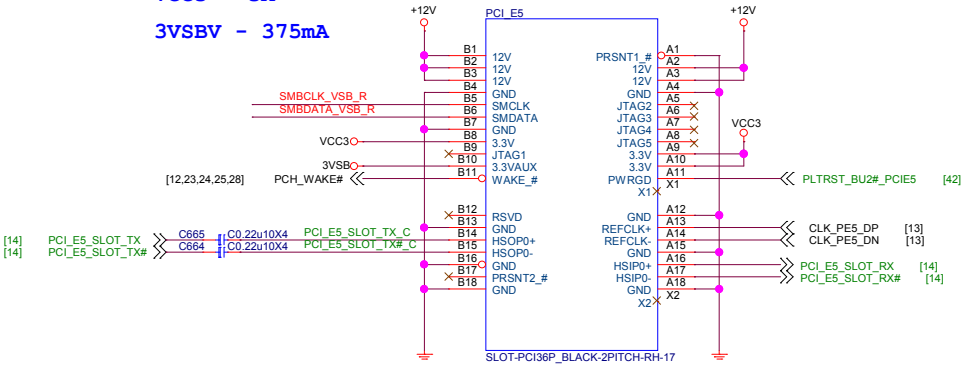
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



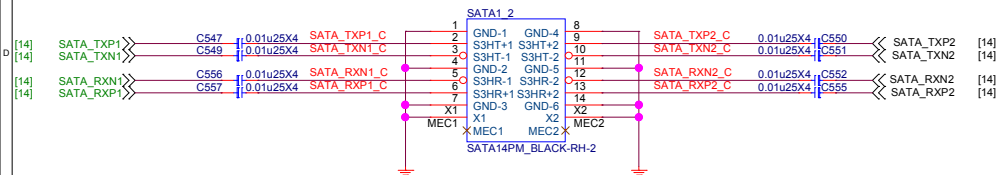
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



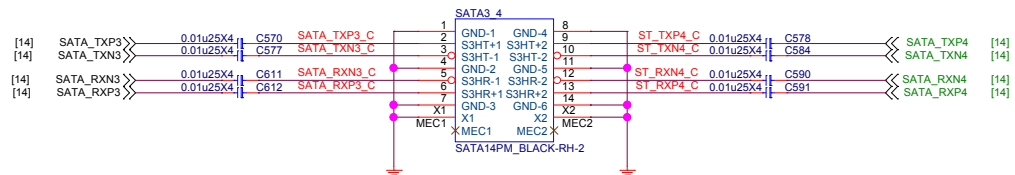
12V - 0.5A
VCC3 - 3A
3VSBV - 375mA



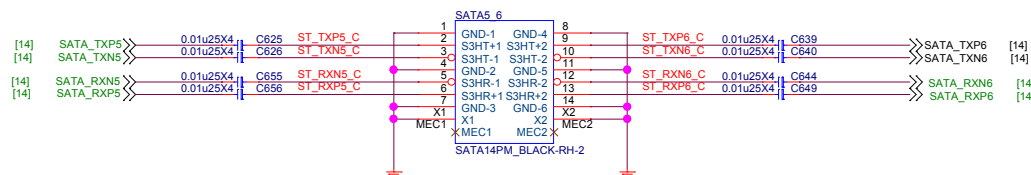
SATA 6G PORT 1.2



SATA 6G PORT 3.4

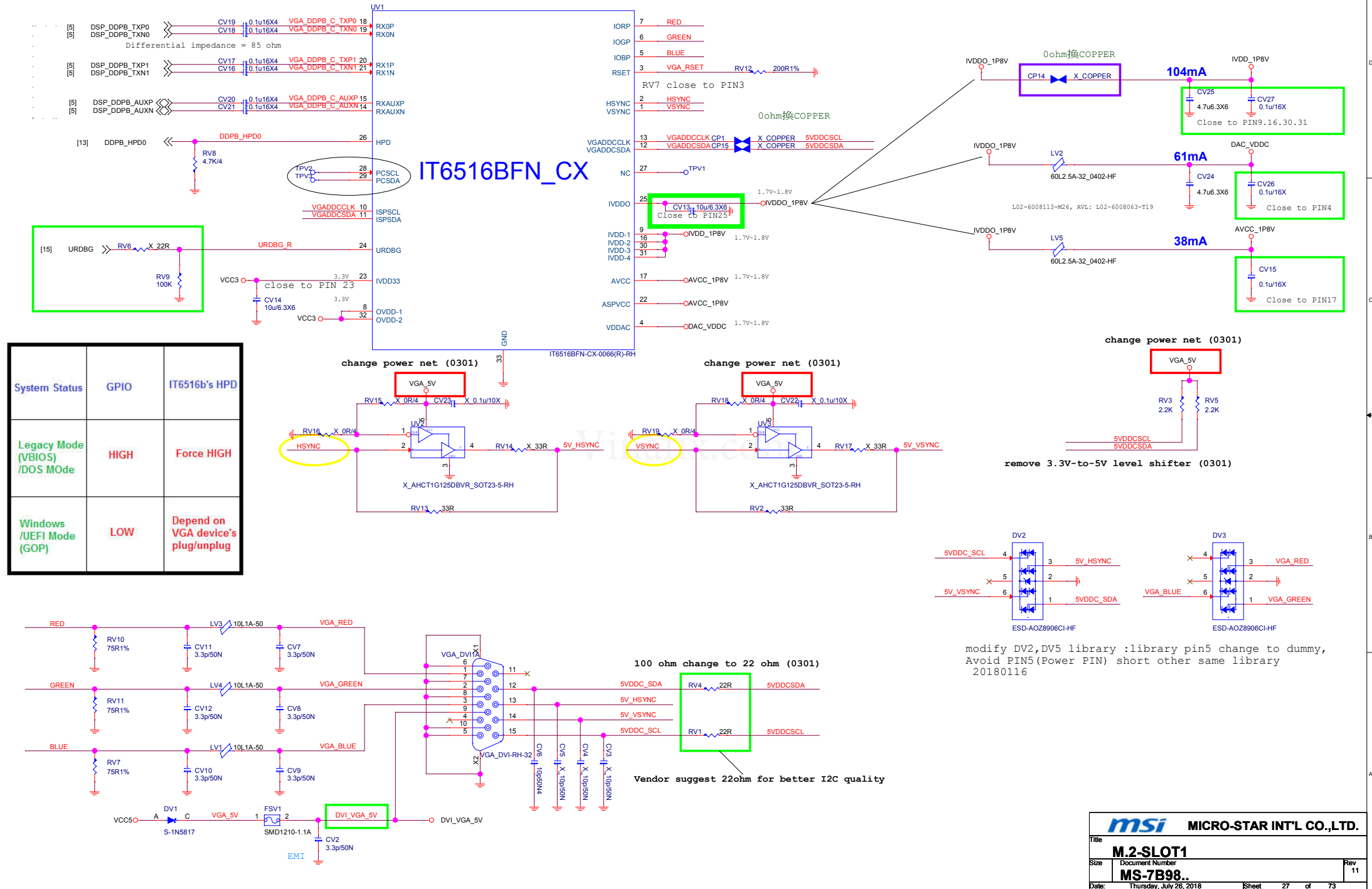


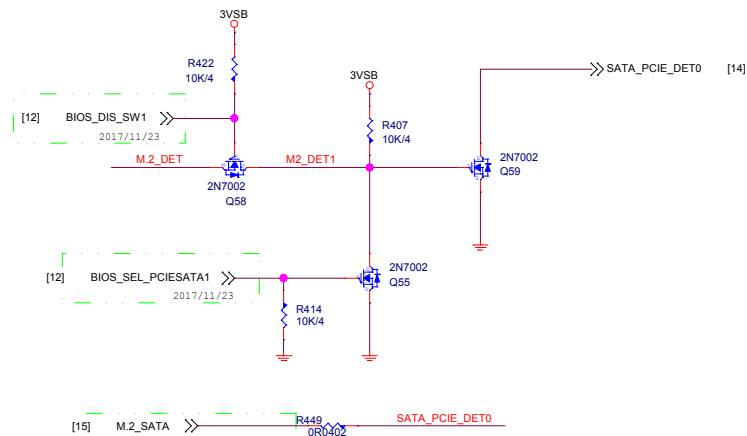
SATA 6G PORT 5.6



Vinafix.com

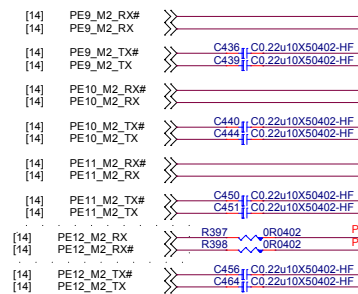
Note:
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



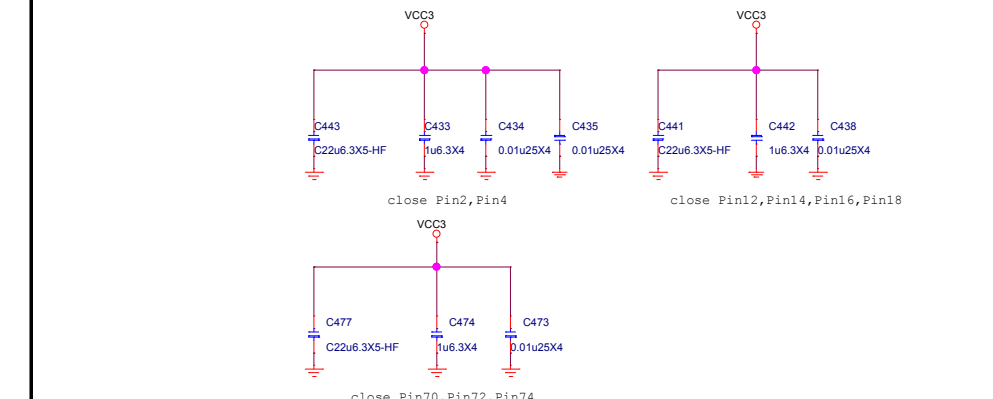
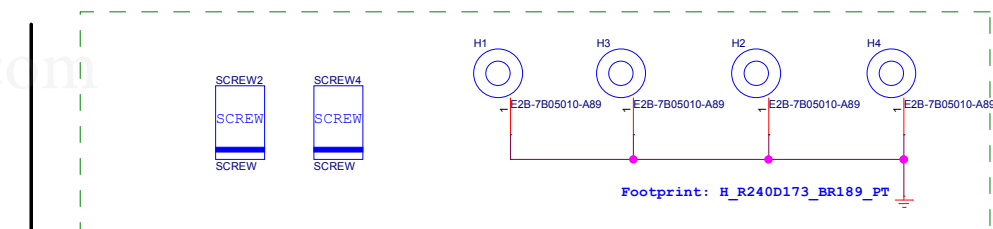


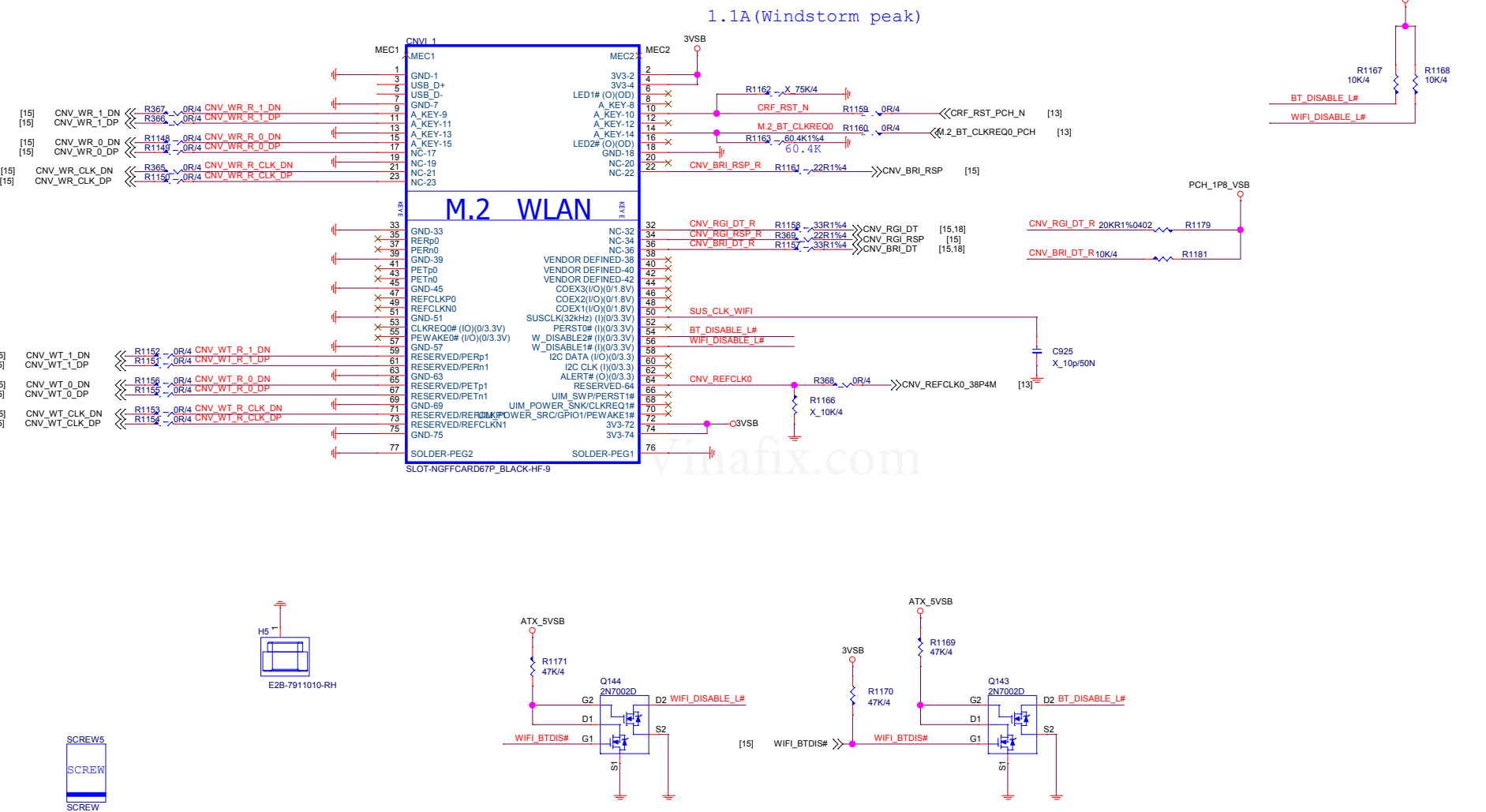
BIOS_MODE

DIS_SW	M1_SEL_PCIESATA	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO



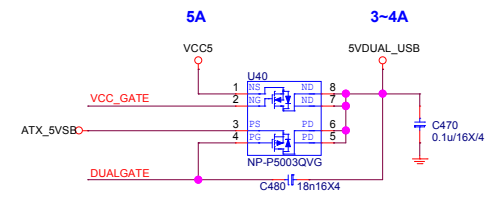
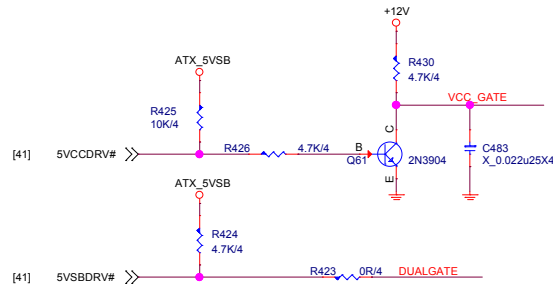
D20,D21 Close to M2 connector



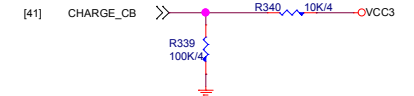


Vinafix.com

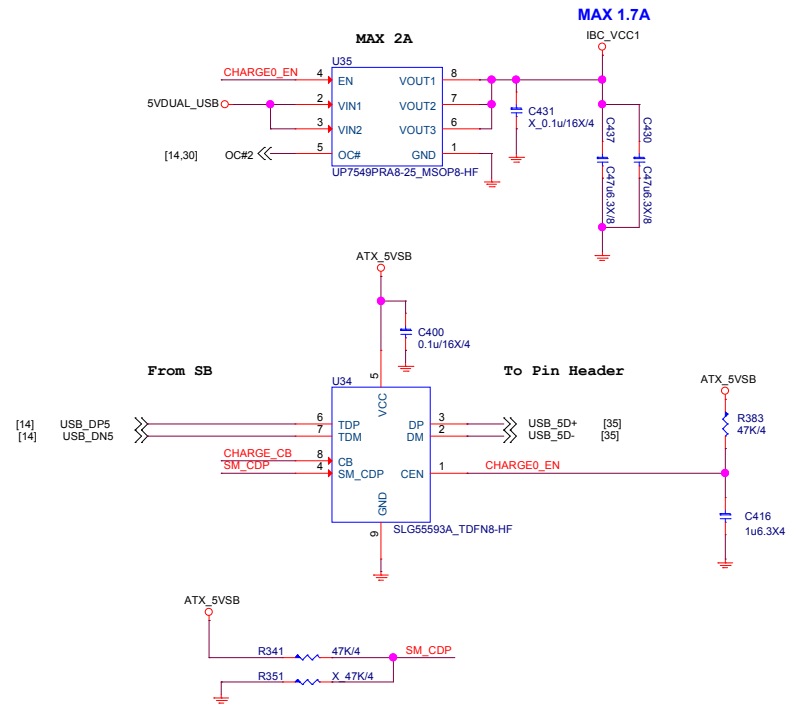
5VDUAL_USB



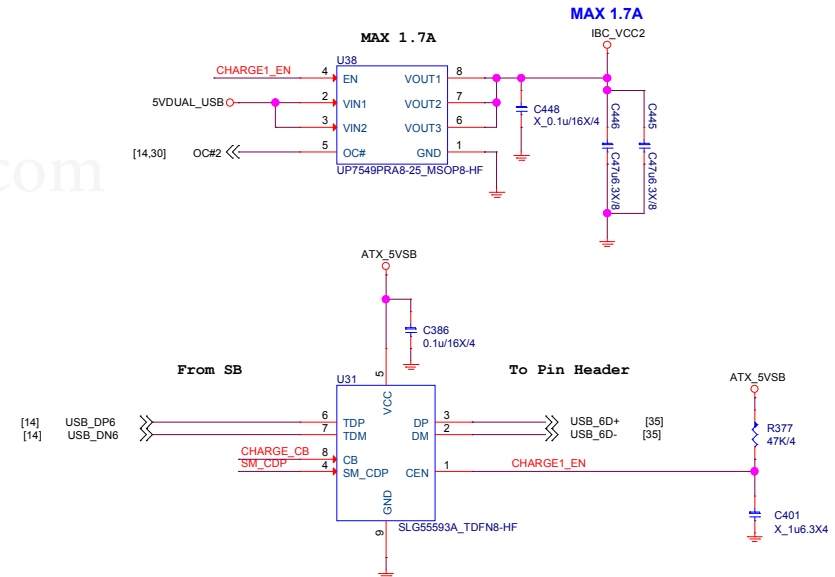
Pin power : I_3VSB
Register power : I_3VSB
Register reset : I_3VSB



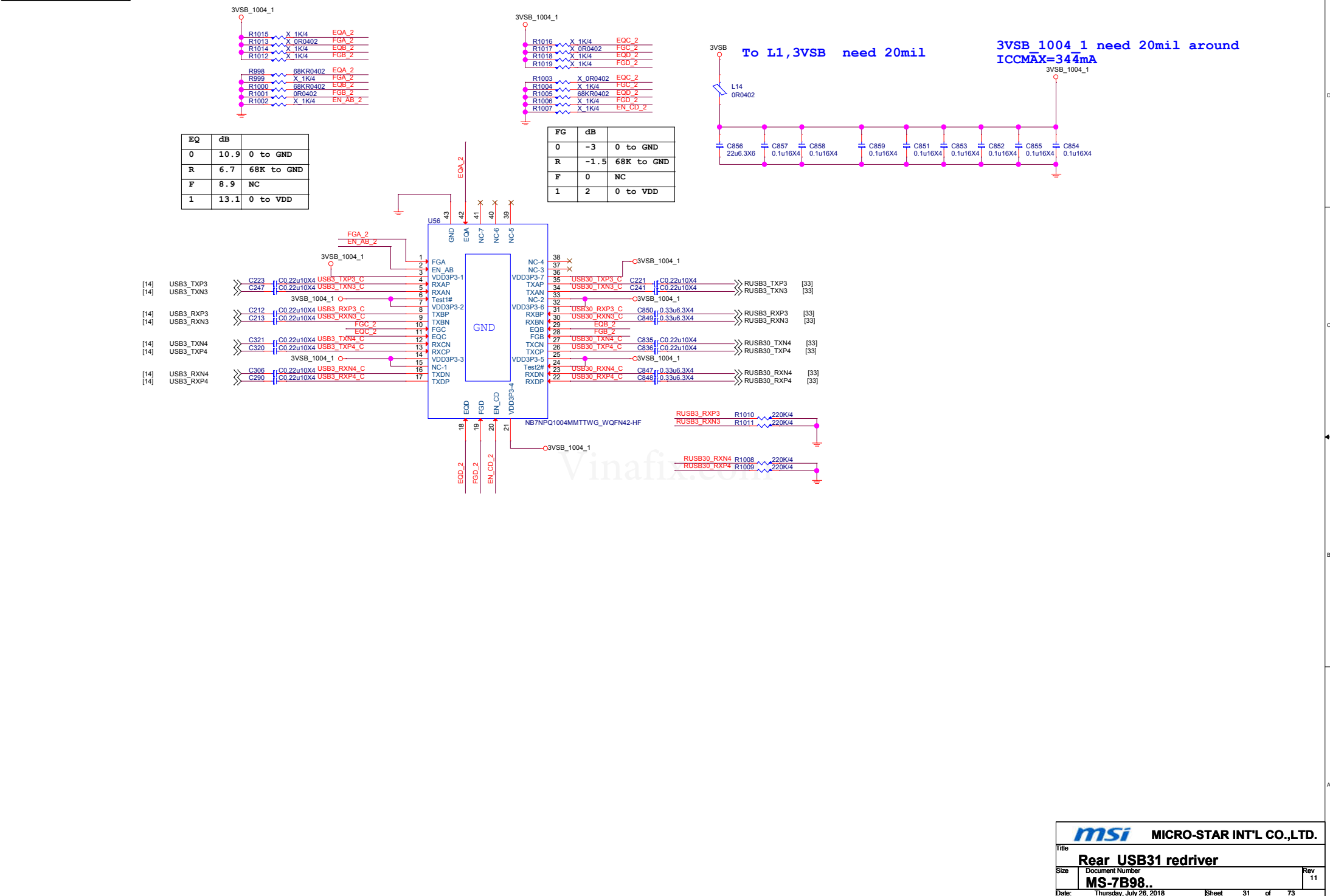
USB POWER PORT 0 For USB Charging



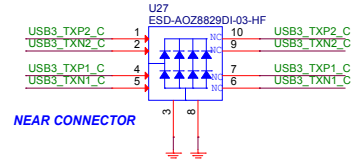
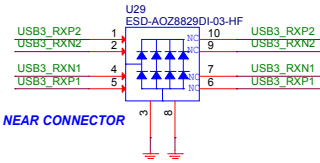
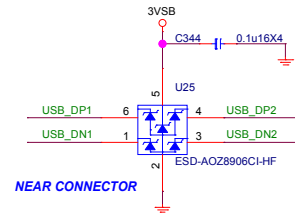
USB POWER PORT 1 For USB Charging



Rear USB3.1 Redriver

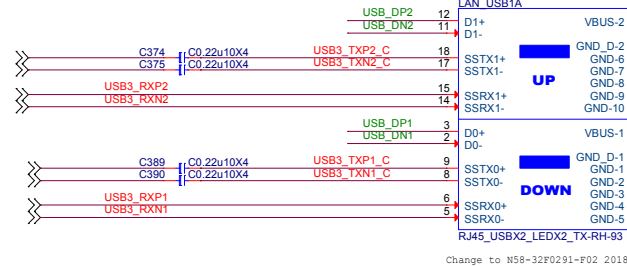


[14] USB_DP2
[14] USB_DN2
[14] USB_DP1
[14] USB_DN1



[14] USB3_TXP2
[14] USB3_TXN2
[14] USB3_RXP2
[14] USB3_RXN2

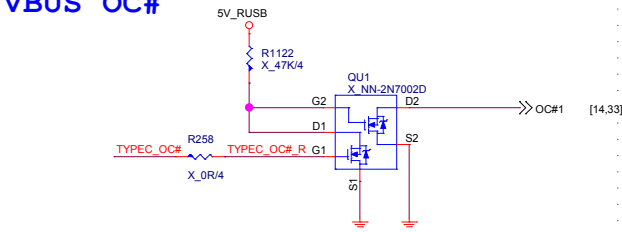
[14] USB3_TXP1
[14] USB3_TXN1
[14] USB3_RXP1
[14] USB3_RXN1



2017/6/22
EC58 is changed from 470uF
to 560uF by buyer request

Vinafix.com

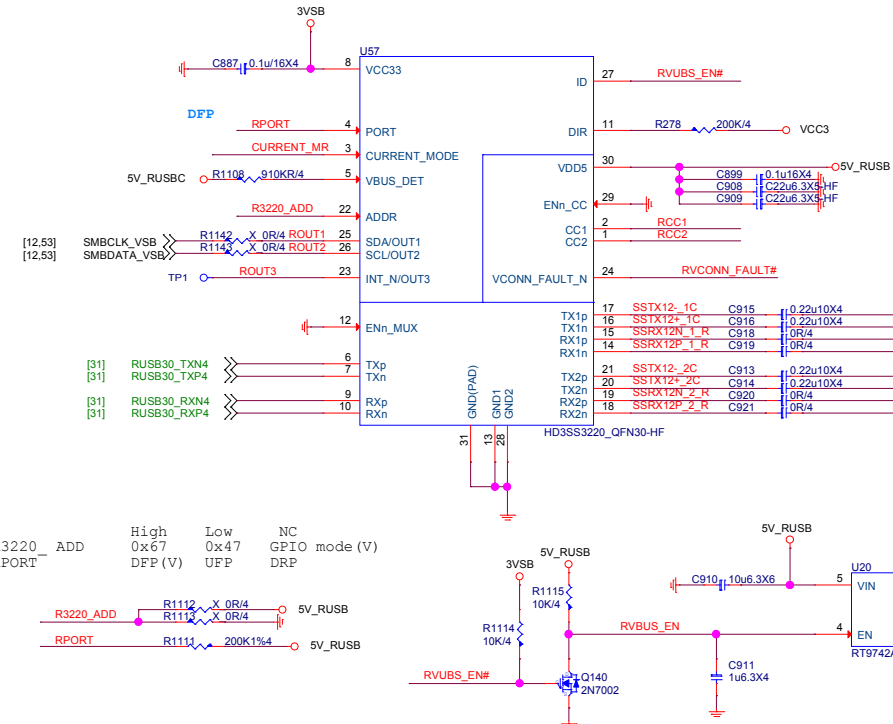
VBUS OC#



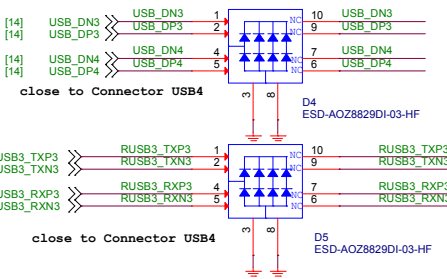
VCONN OC#



USB Type-C MUX with Configuration Channel (CC)

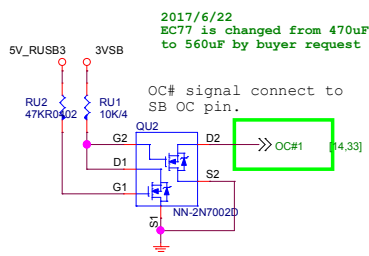
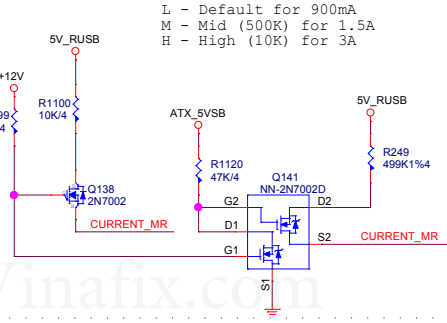


3 A
min 80mil.

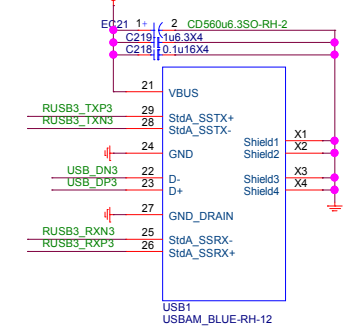


Current Mode

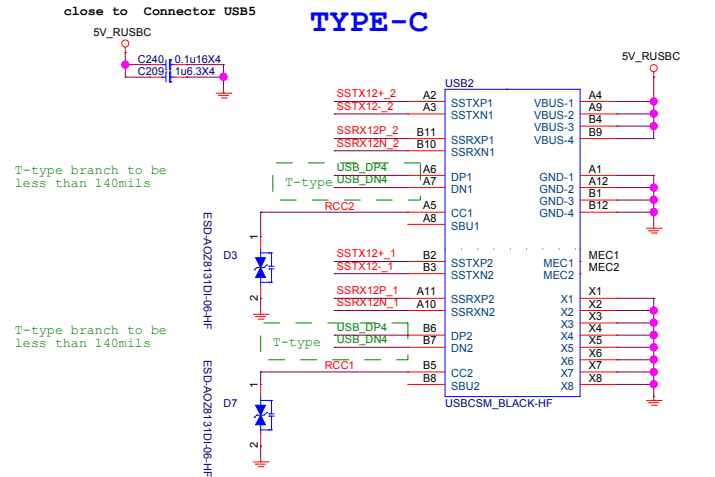
3A under S0 mode
1.5A under S3 mode



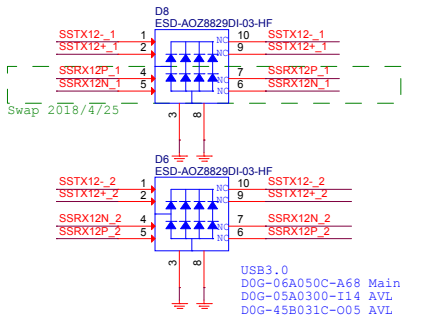
TYPE-A



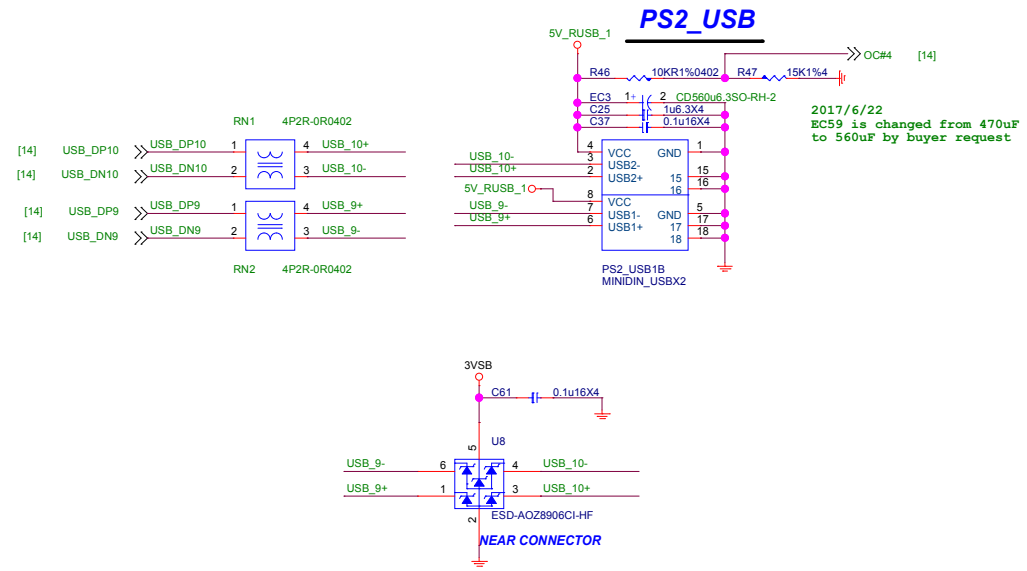
TYPE-C



ESD Protection NEAR AC CAP

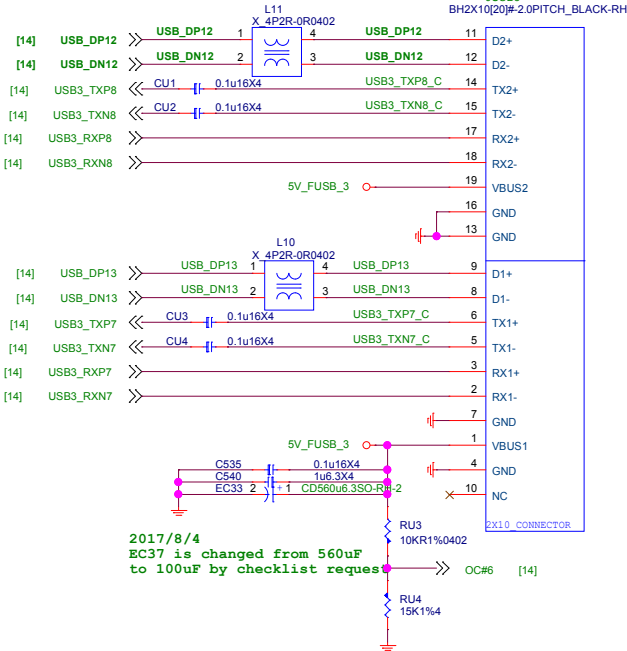


REAR USB2.0



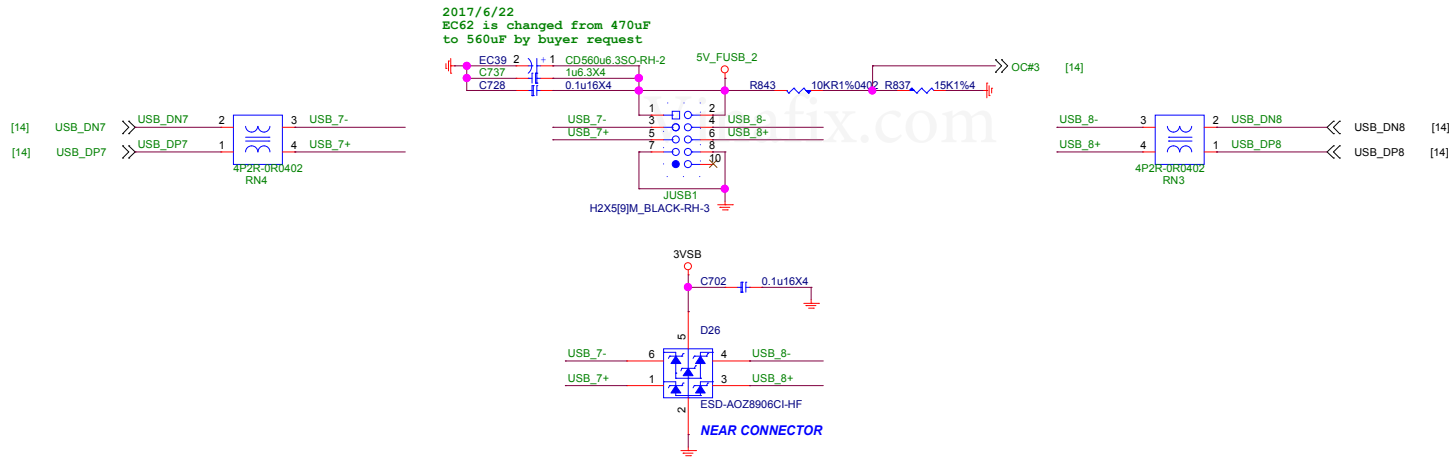
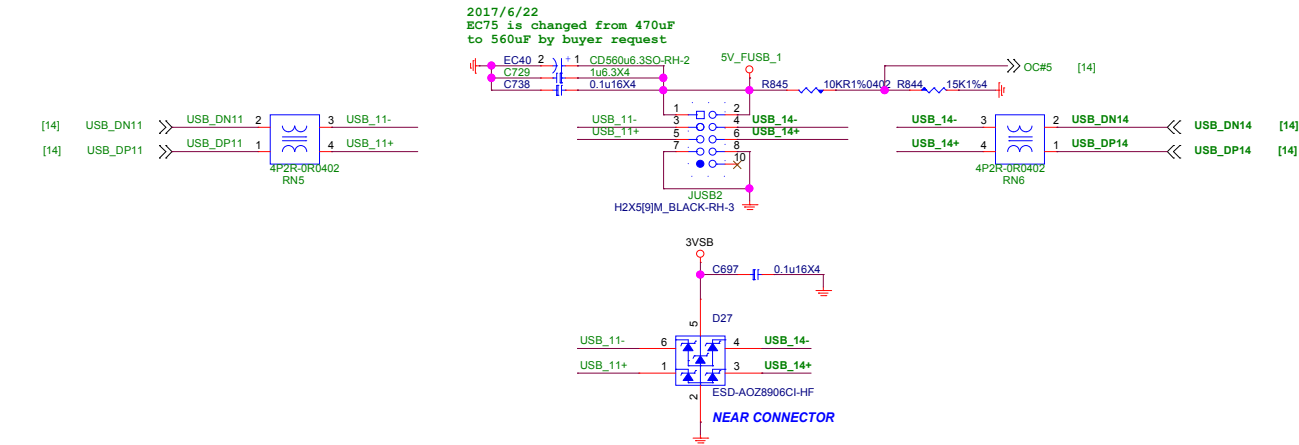
Vinafix.com

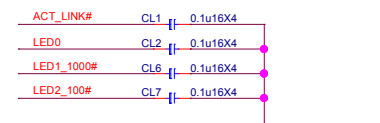
B SKU 不上件



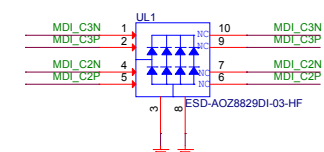
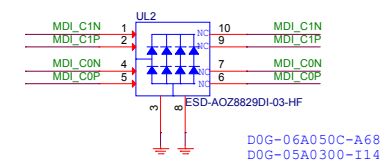
The schematic diagram illustrates the USB interface for the BH2X10[20]-2PITCH_BLACK-RH-A module. It features two USB connectors, USB4 and USB5, connected to the module's internal components. USB4 is connected to the L3 4P2R-0R0402 component, which is connected to the USB3_TXP6, USB3_TXN6, USB3_RXP6, and USB3_RXN6 pins. USB5 is connected to the L5 4P2R-0R0402 component, which is connected to the USB3_TXP5, USB3_TXN5, USB3_RXP5, and USB3_RXN5 pins. The diagram also shows the connection of IBC_VCC1 and IBC_VCC2 to the module's power pins. The module is connected to a 2x10 connector with pins D2+, D2-, TX2+, TX2-, RX2+, RX2-, VBUS-2, GND-1, GND-2, D1+, D1-, TX1+, TX1-, RX1+, RX1-, GND-3, VBUS-1, GND-4, and NC.

FRONT USB2.0





UL2&UL3 close to connector

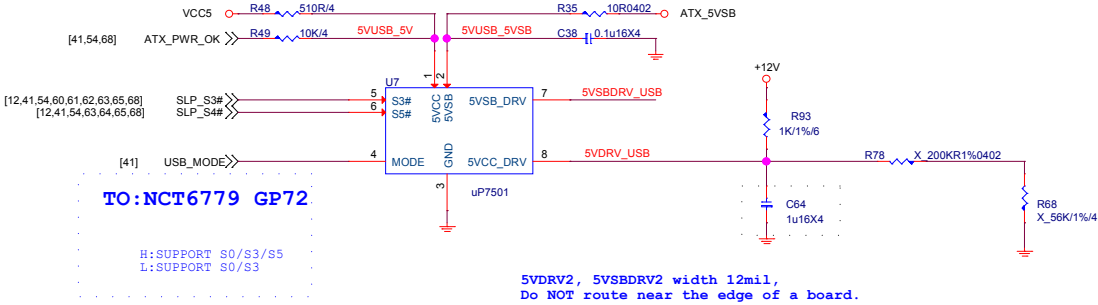


+3.3V LAN

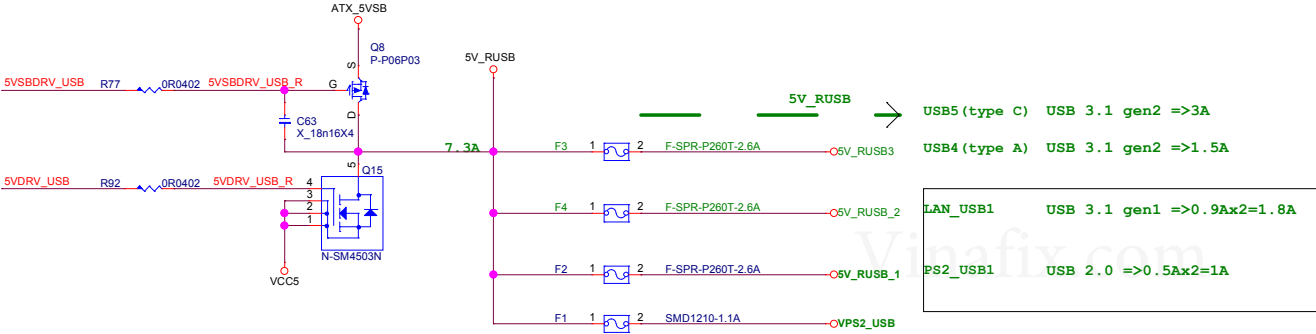
I219:542mW

Note: These caps closed to PHY

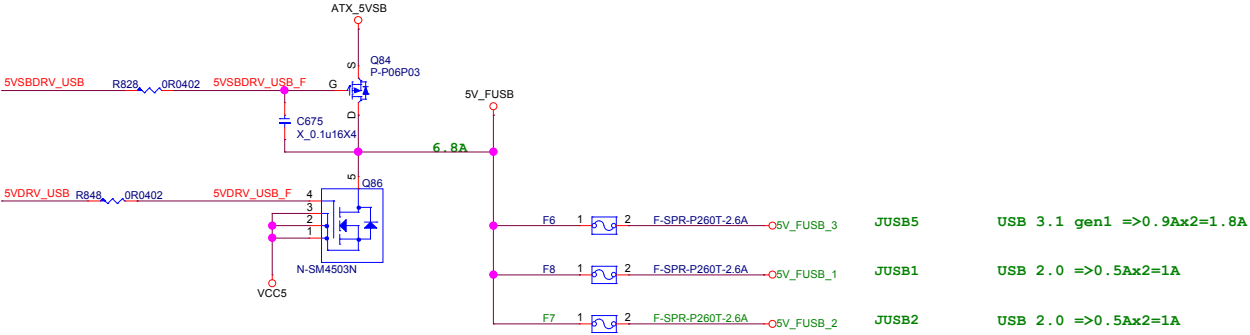
USB POWER



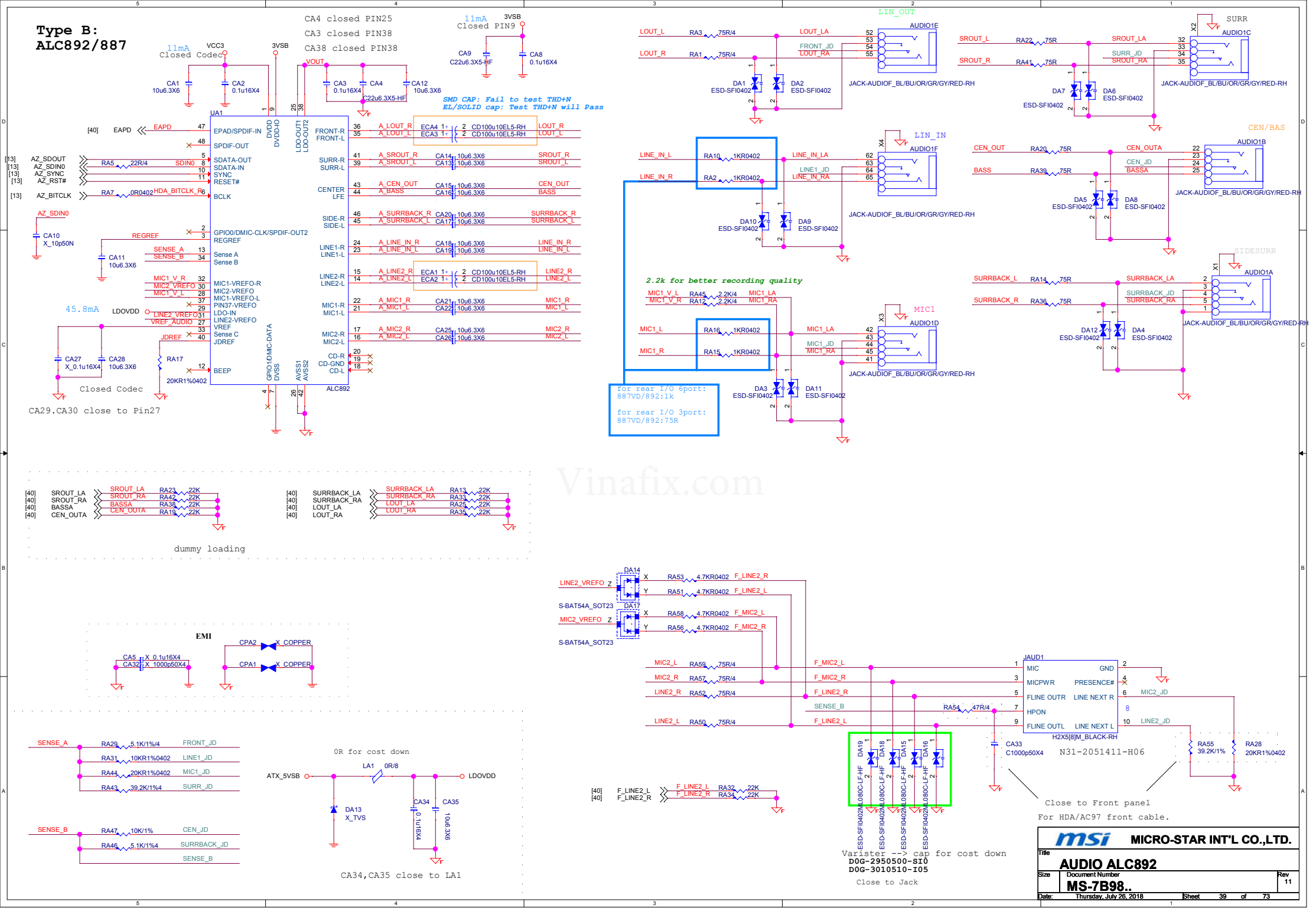
REAR USB PORT POWER



FRONT USB PORT POWER



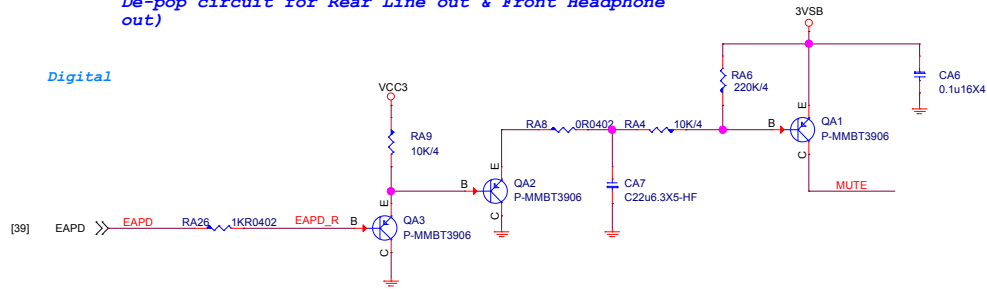
Type B: ALC892/887



Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

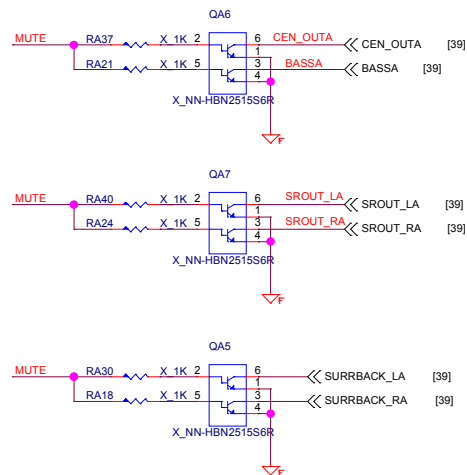
Digital

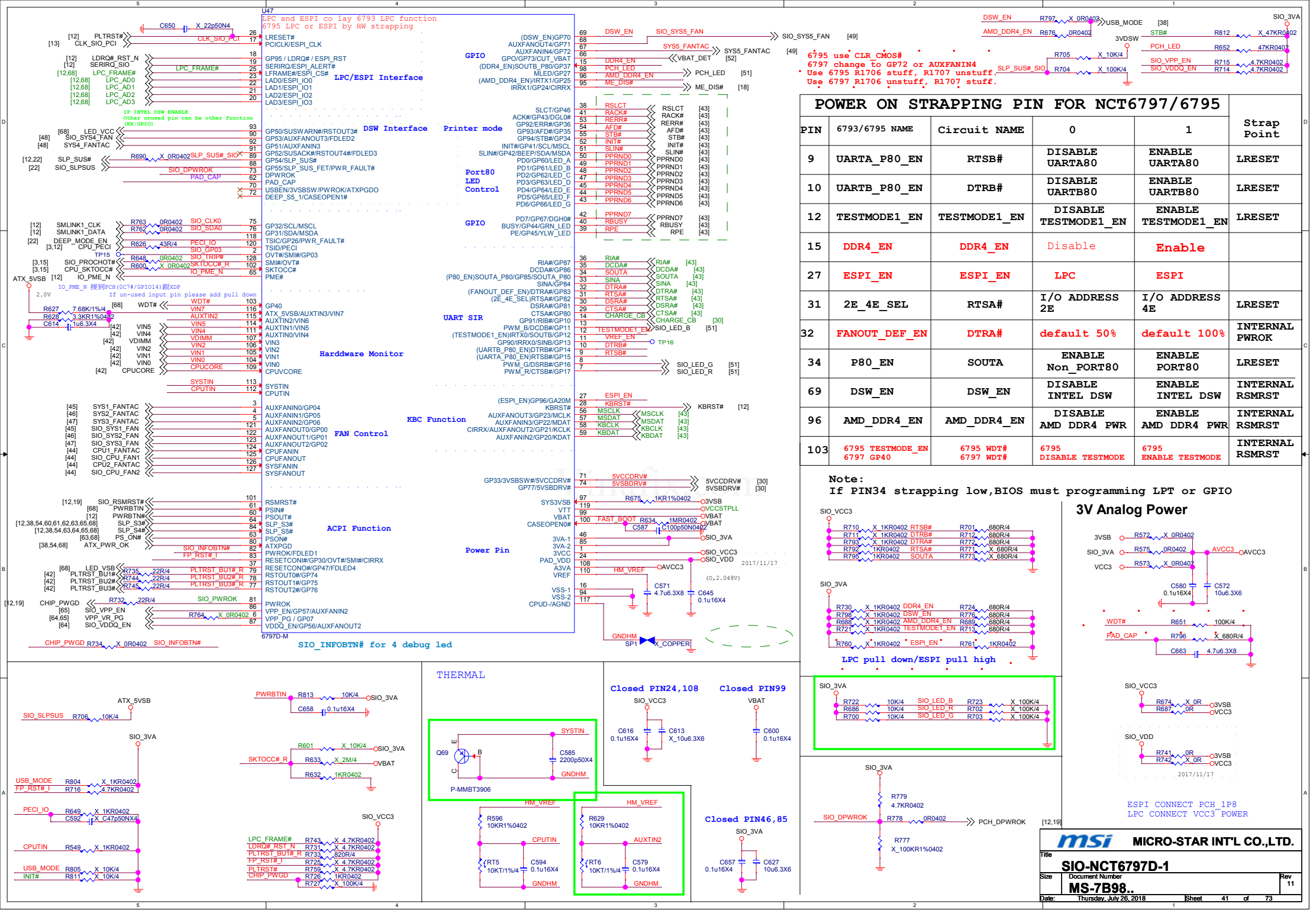


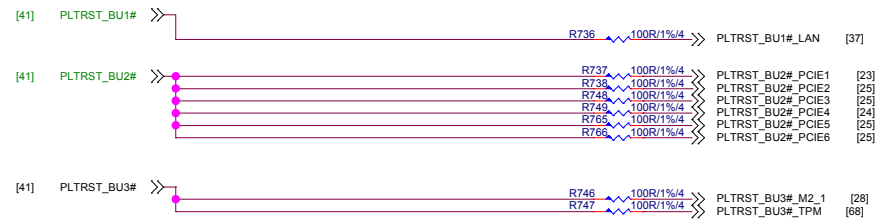
Analog



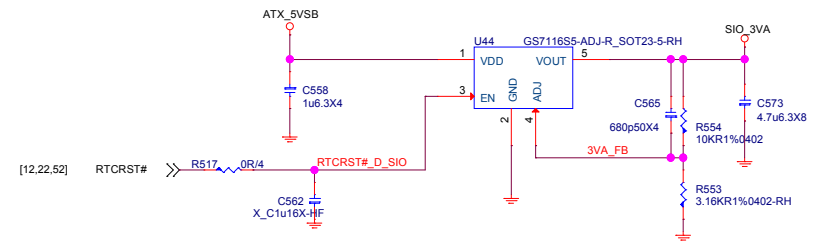
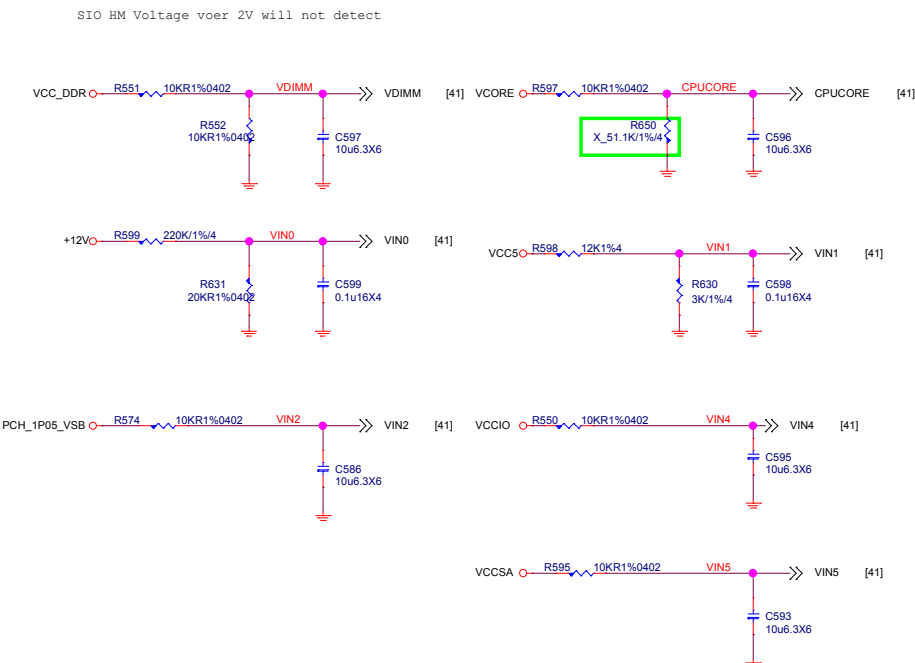
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5,CA11, CA12, CA13, CA21, CA22 to TVS)





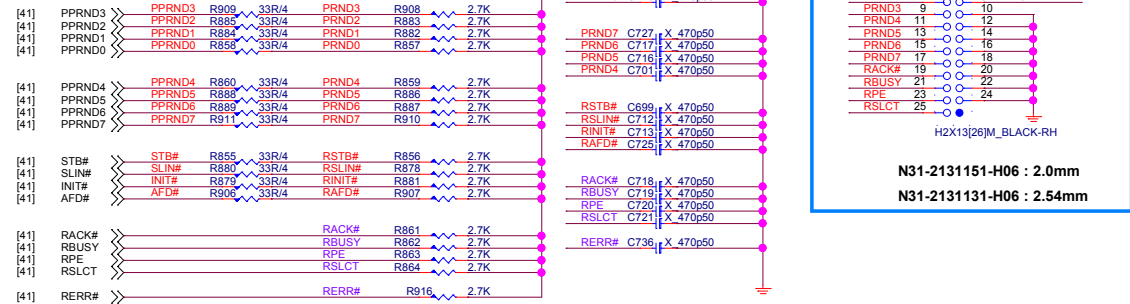
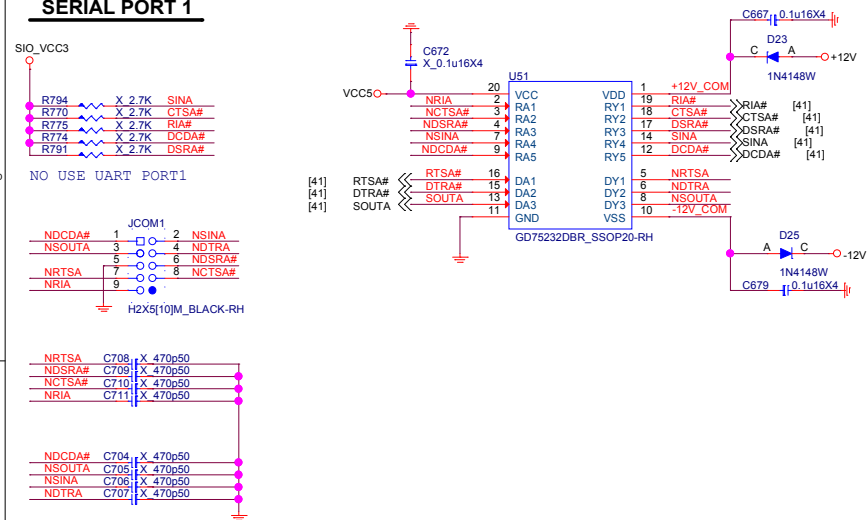


HW Monitor - Voltage



SERIAL PORT 1

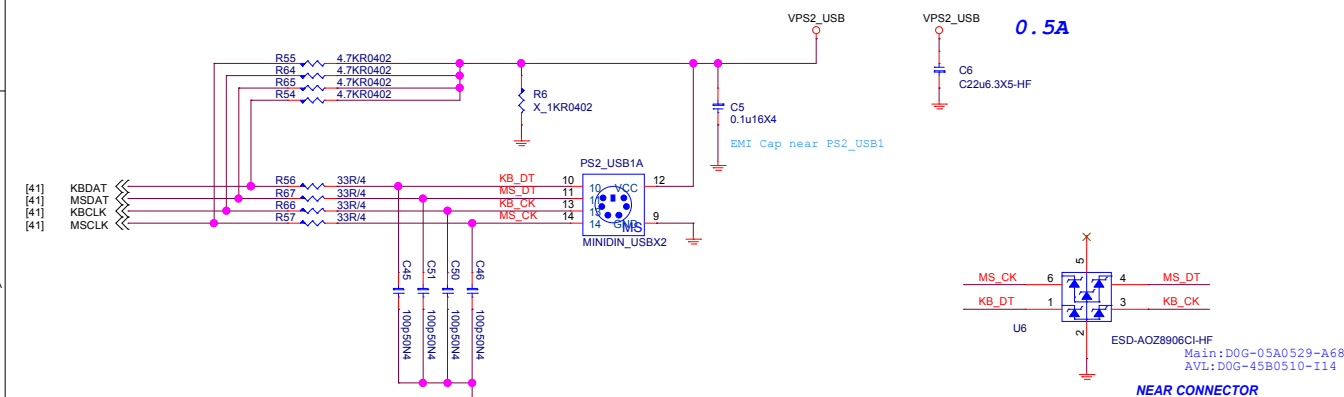
PARALLAL PORT



PS2 KEYBOARD & MOUSE CONNECTOR

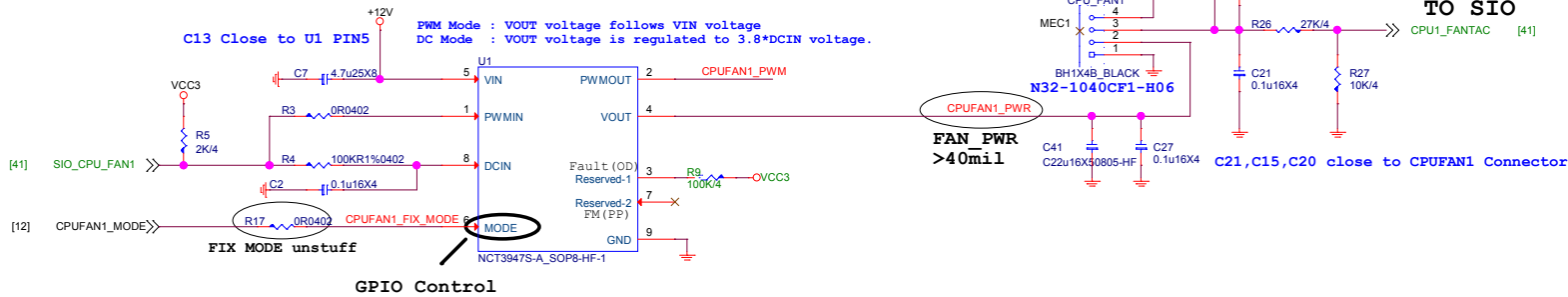
PS2 Power

Vinafix.com



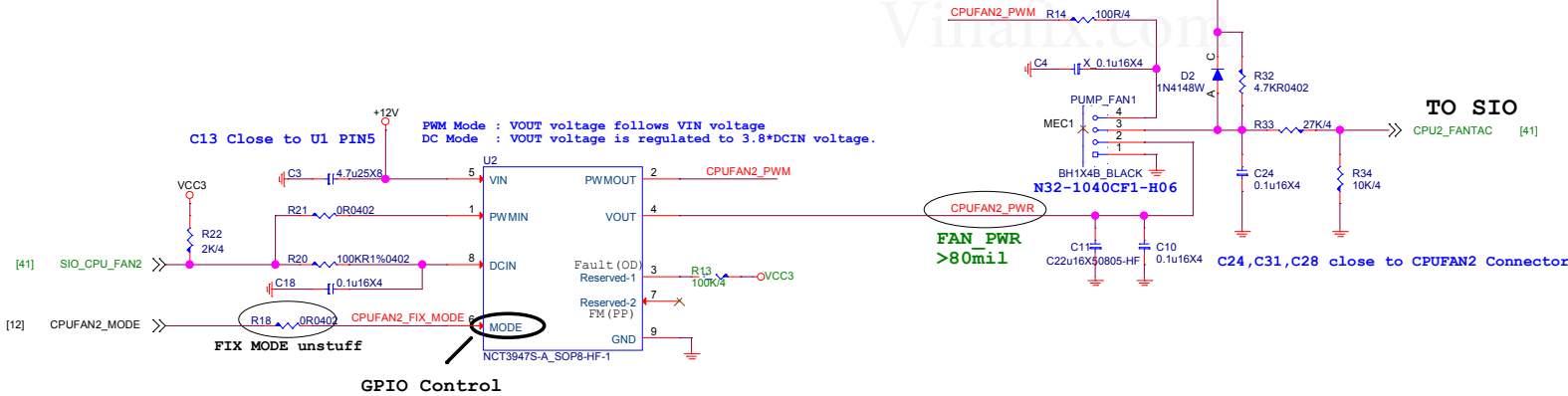
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

- 1.PWM/DC/OCF LED (R/G/B3 LED)
- 2.GPIO BIOS PWM/DC MODE
- 3.OCF GPIO BIOS
- 4.PWM OR DC FAN GPIO BIOS
- 5.FAN 時 SOFTWARE GPIO



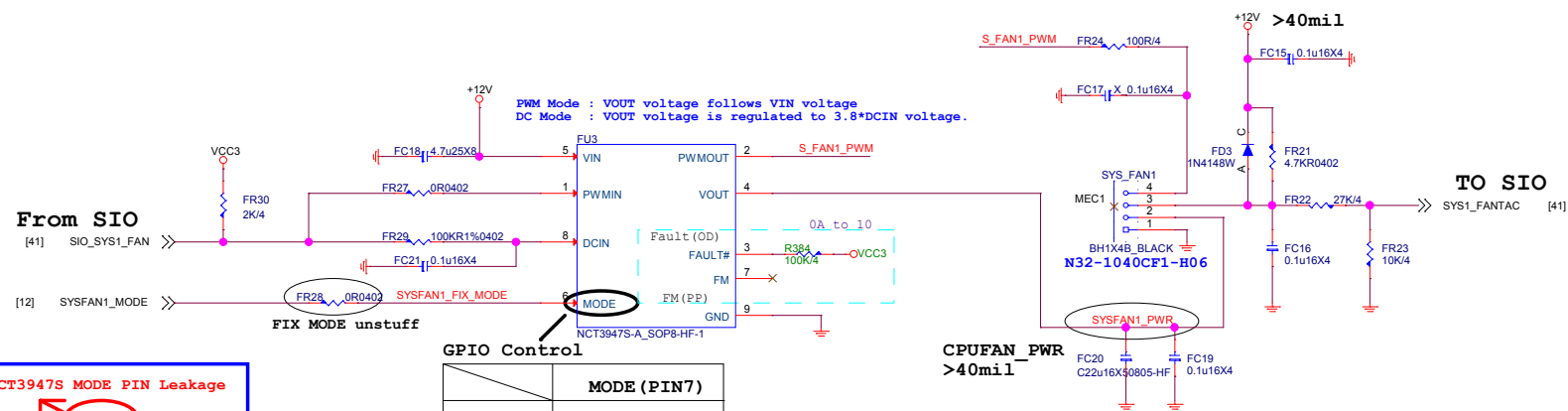
Vinafix.com

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

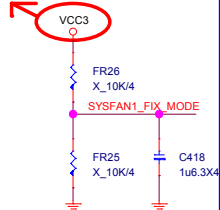


- 1.MODE : USE MODE PIN change FAN MODE(PWM or DC FAN)
- 2.FAULT : USE FAULT PIN Triger OVT/OCF Protection,LOW Atcive (Reserve NEW IC)
- 3.FM : USE FM PIN For BIOS USE to Detect PWM or DC FAN & Show information(Reserve NEW IC)

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



Avoid NCT3947S MODE PIN Leakage



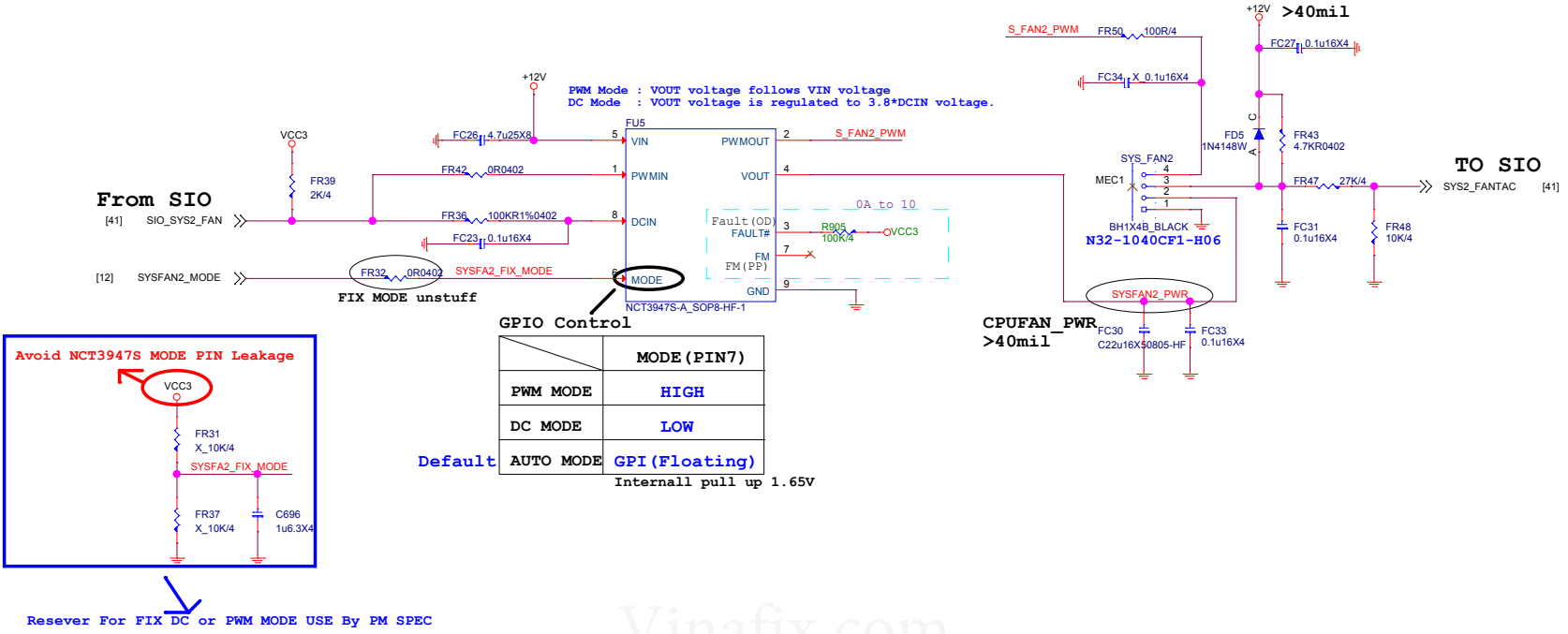
Resever For FIX DC or PWM MODE USE By PM SPEC

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default

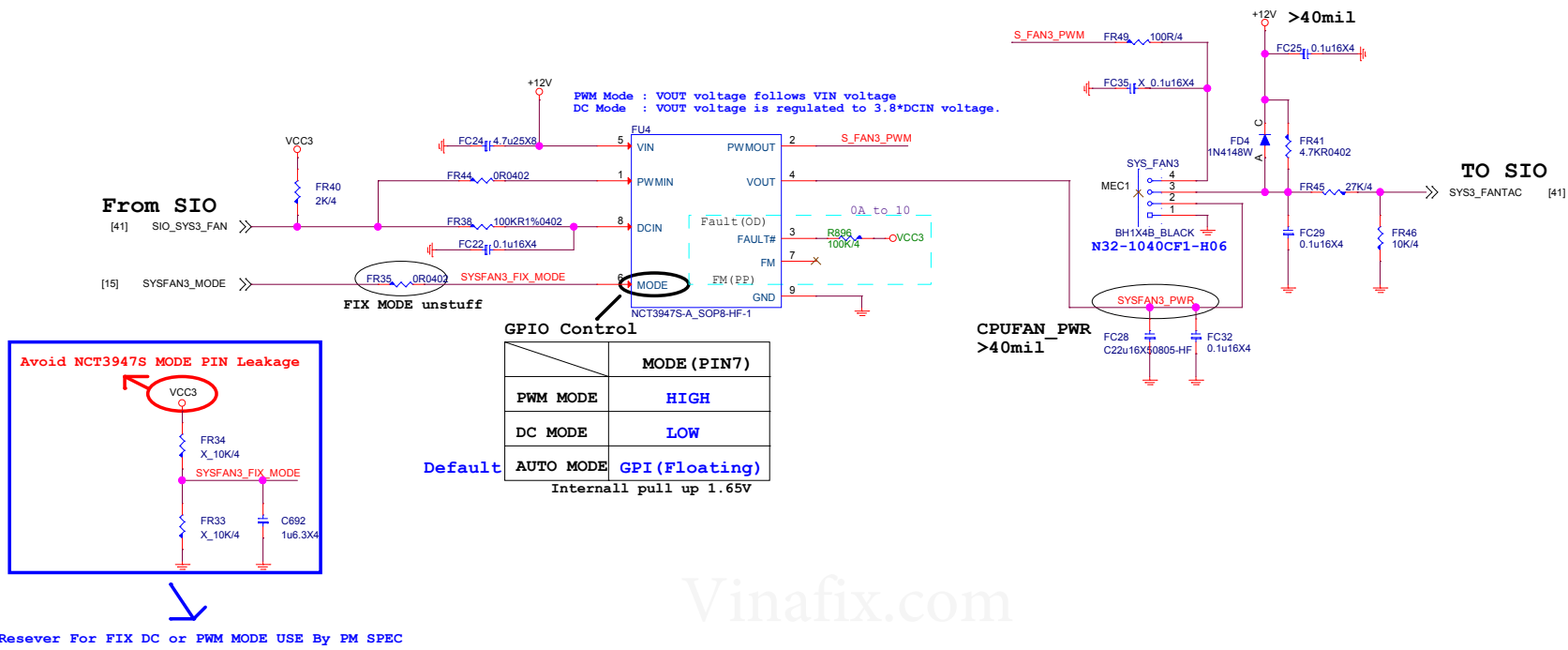
Internall pull up 1.65V

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



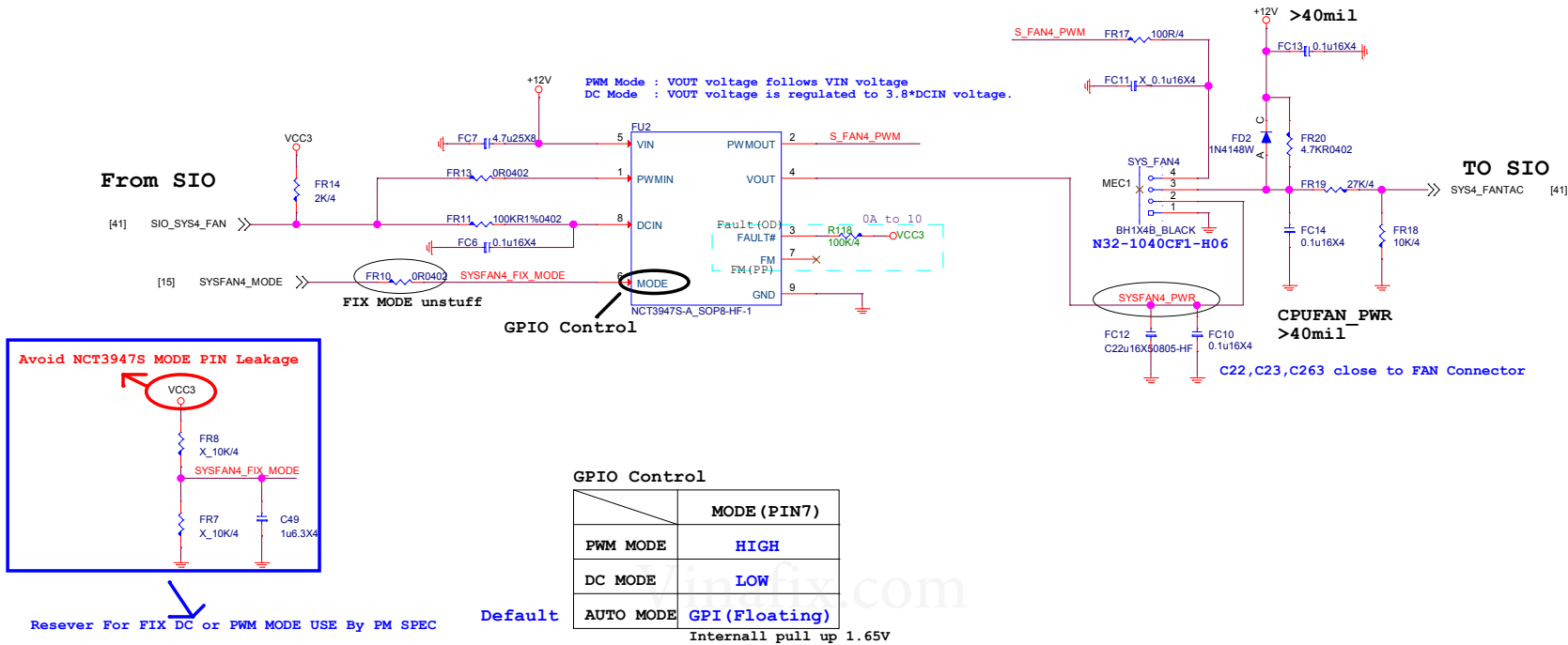
Vinafix.com

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

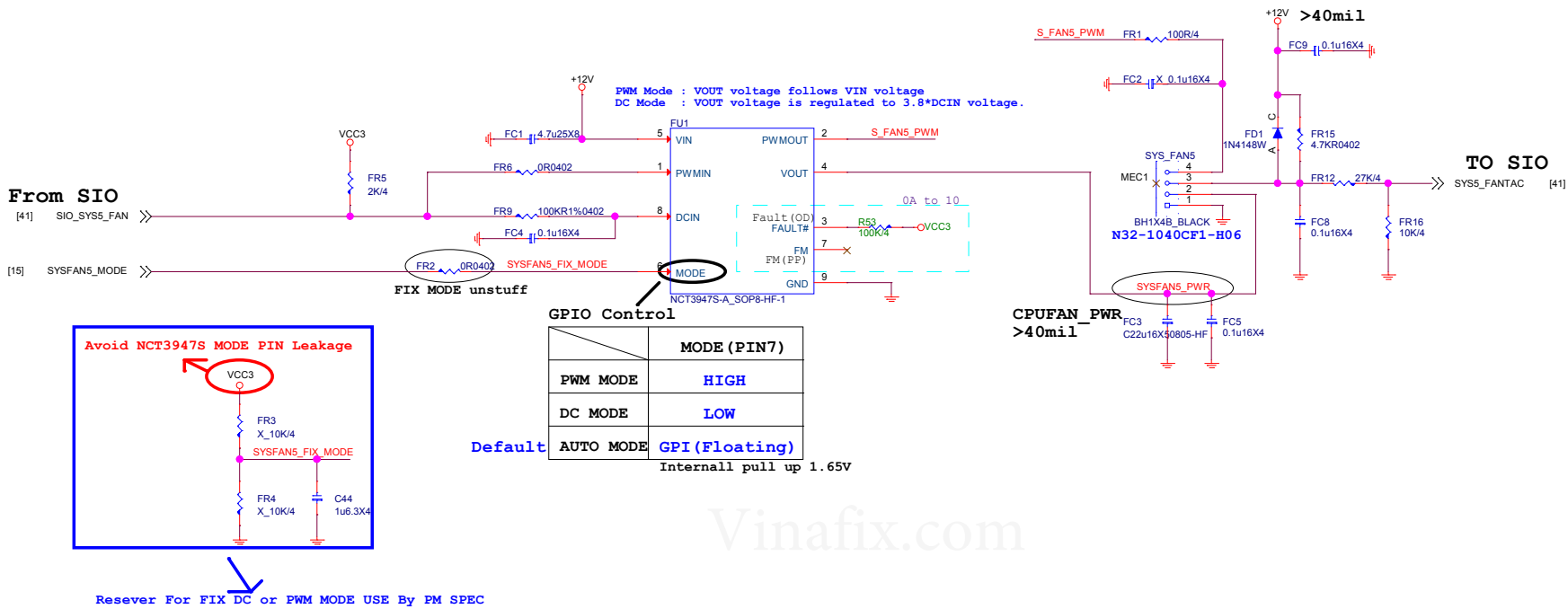


TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

2.GPIO可以由BIOS切换 PWM/DC MODE



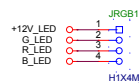
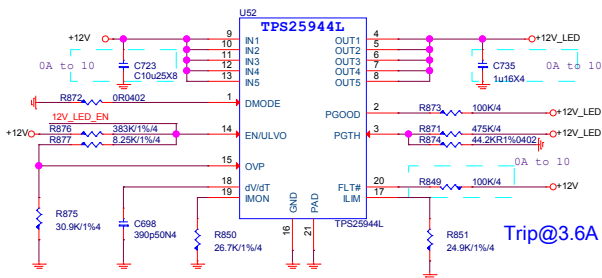
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



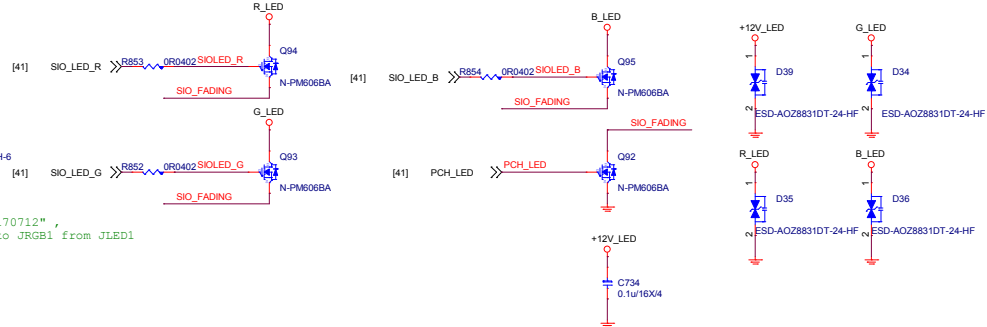
Delete ALL Audio LED BY Spec Change 2018/4/19

Vinafix.com

JLED



2017/7/28
Based on "MSI-Header_20170712",
pin header(1x4) change to JRGB1 from JLED1

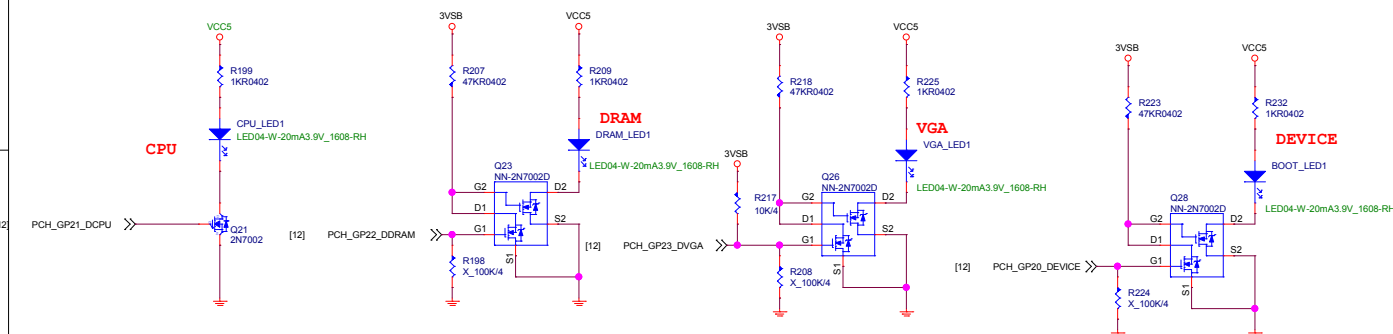


Delete ALL Audio LED BY Spec Change 2018/4/19

Vinafix.com

EZ DEBUG

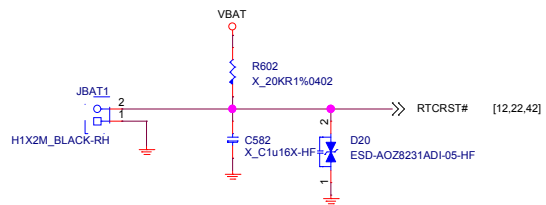
白 : M:D0C-040T200-H91/ S:D0C-040S200-E07*4



GPIO LED	PCH_GP20	PCH_GP21	PCH_GP22	PCH_GP23
亮	NATIVE PULL HIGH	GPO PULL HIGH	GPO PULL HIGH	NATIVE PULL HIGH
滅	NATIVE LOW	GPO LOW (default LOW)	GPO LOW (default LOW)	GPO LOW (default LOW)

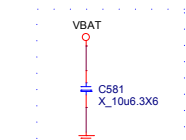
關機斷電狀態下，4個LED先維持default全暗，開機通電後：

1. 首先進行CPU check CPU LED 亮，check PASS後則CPU LED減掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED減掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED減掉。
4. 因此最後正常順利開機後，三個LED燈都是減掉的。
(系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作)

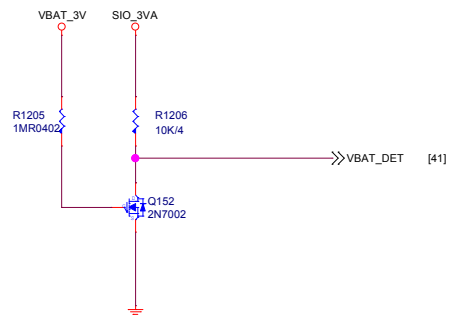
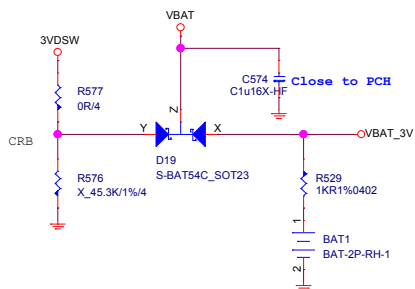


Vinafix.com

VBAT



have timing issue keep
0805 size don't removed



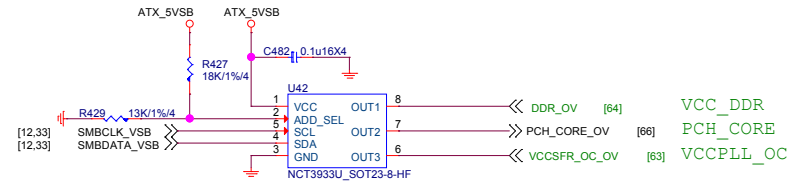
UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

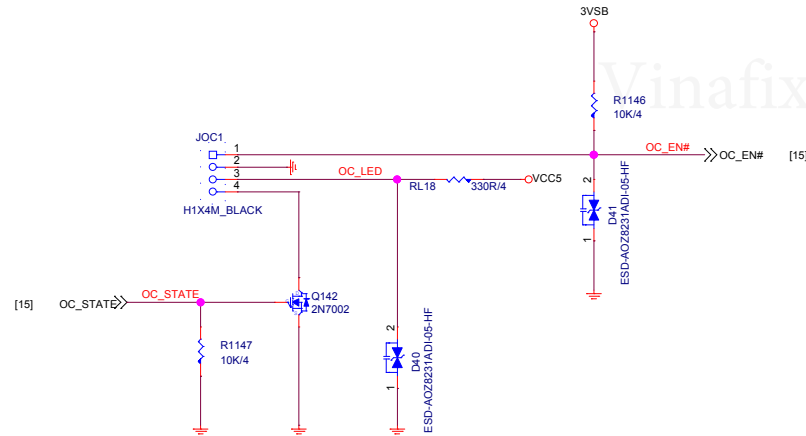
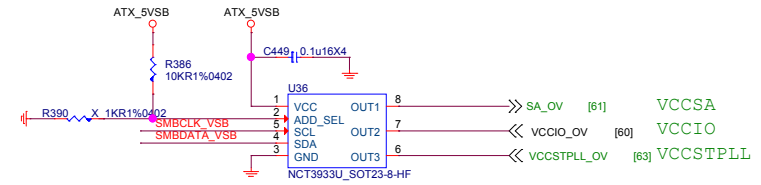
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K

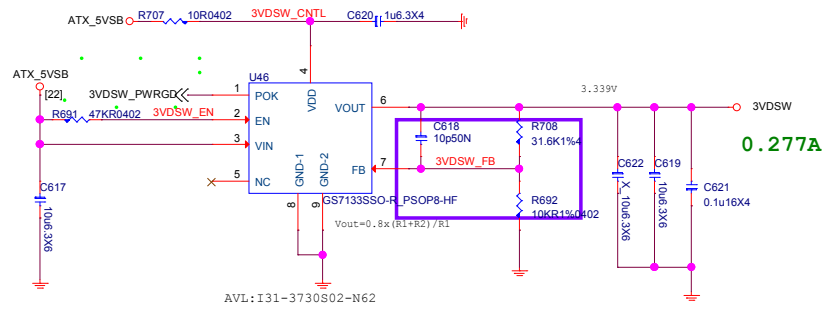


UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

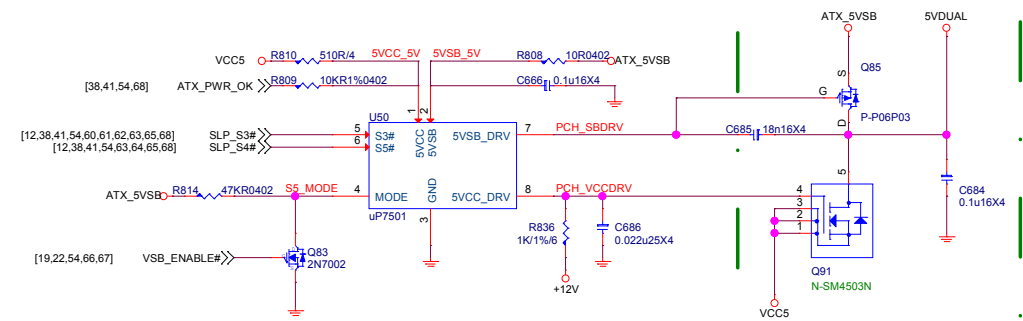


3VDSW



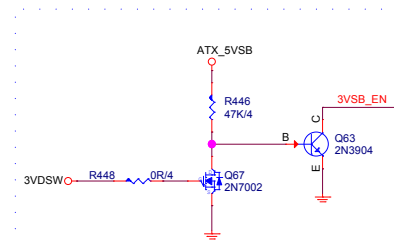
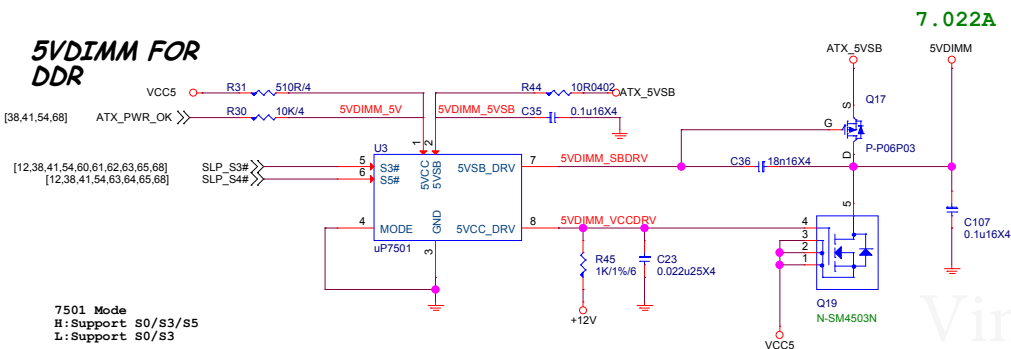
5VDUAL

5VDUAL is power source of 1P0SB



Change to discrete type
2018/1/18

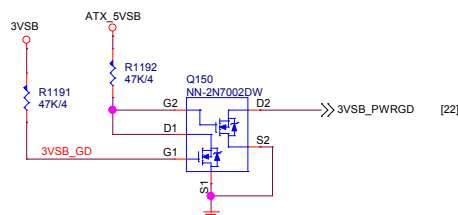
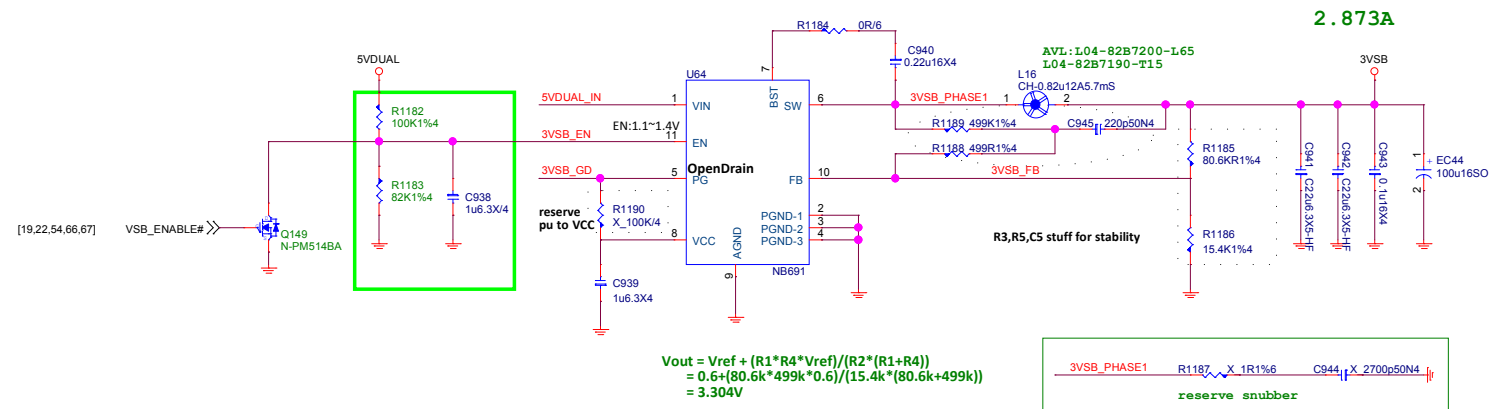
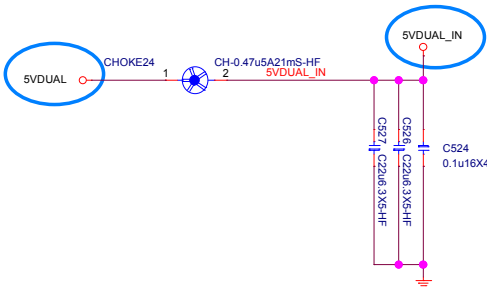
5VDIMM FOR
DDR

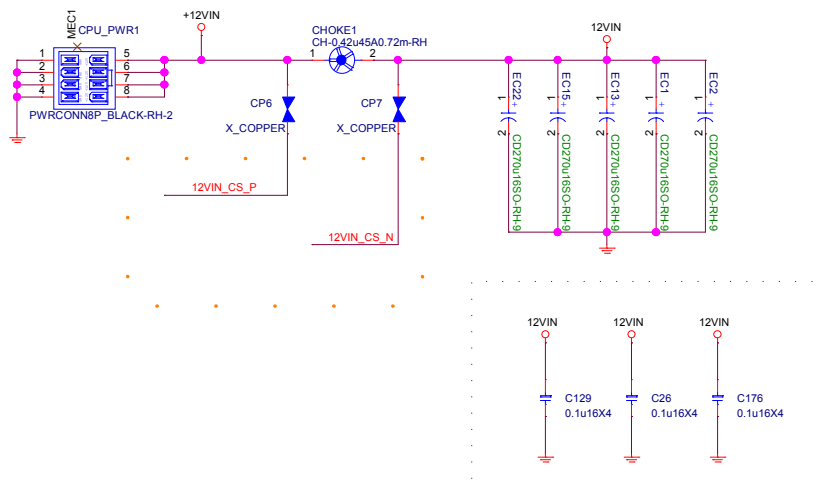
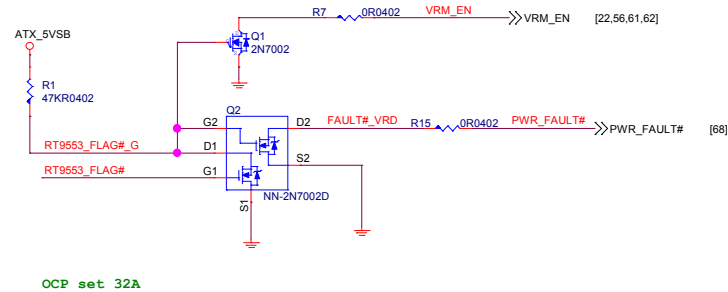
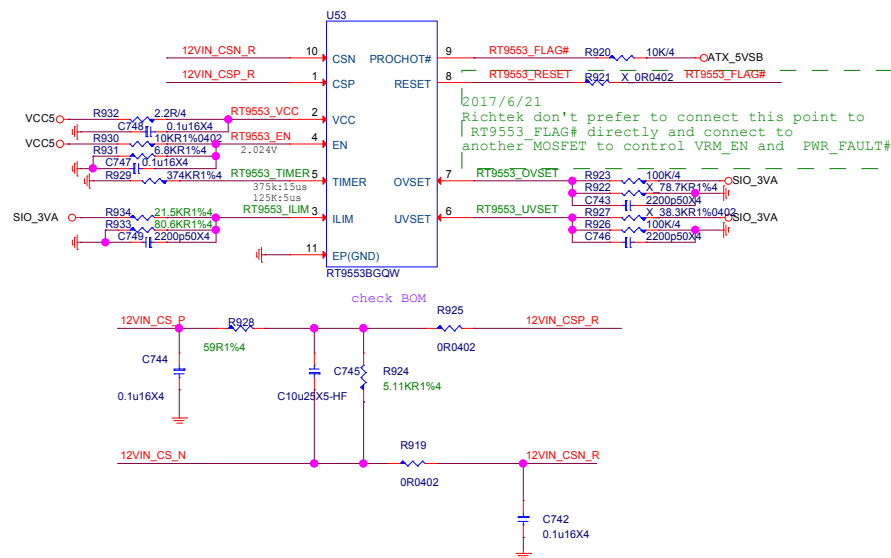


for S5-G3 3VSB_EN ISSUE

$$L = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$
$$= 0.8311 \mu H \text{ (K = 30\%)}$$
$$L = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$
$$= 0.4987 \mu H \text{ (K = 50\%)}$$

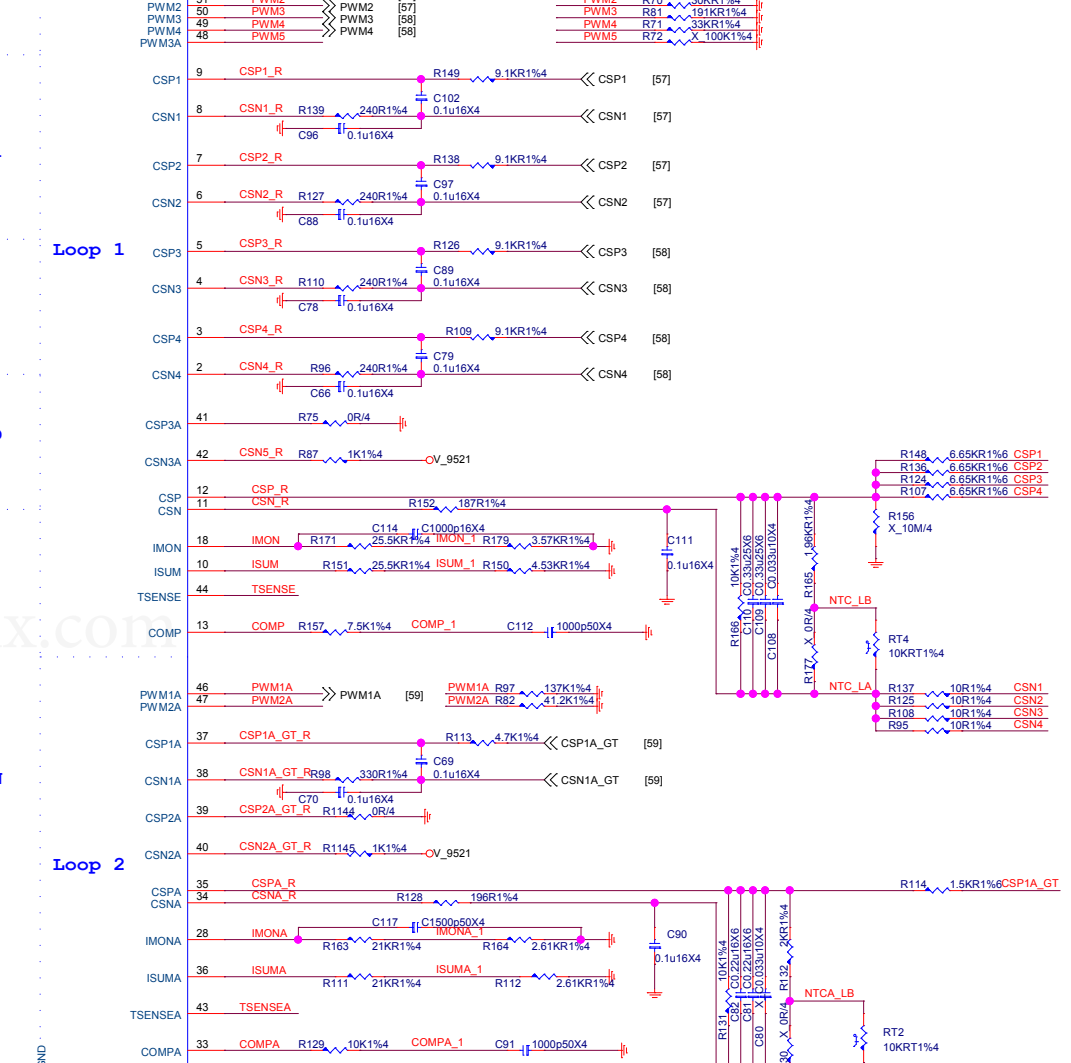
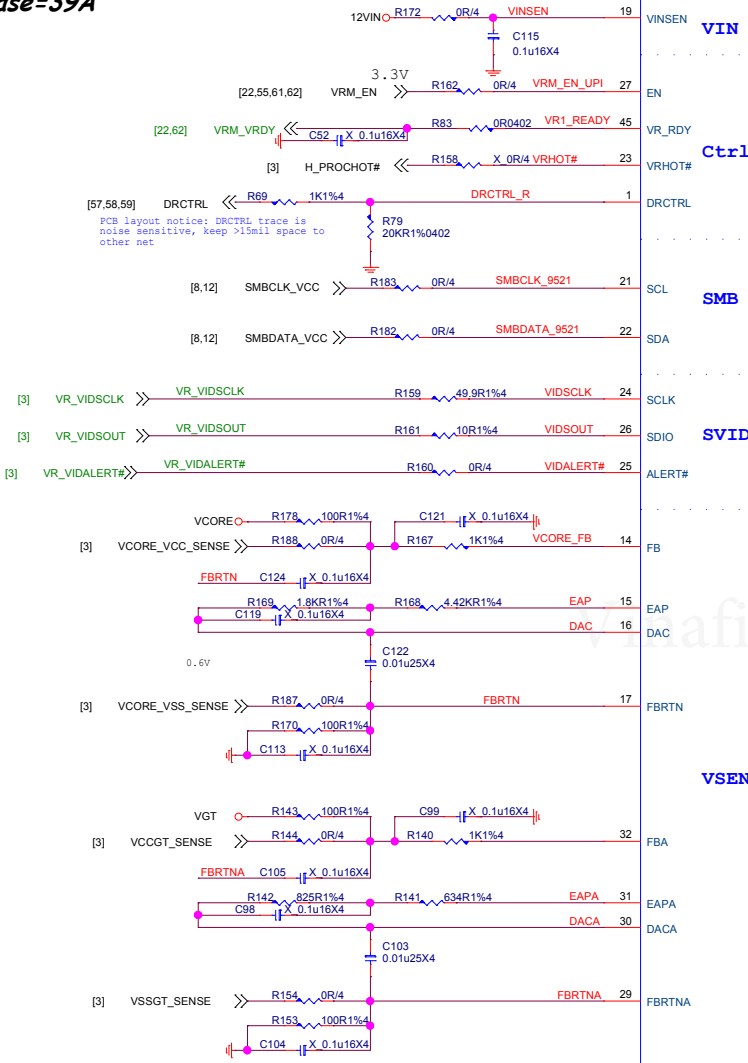
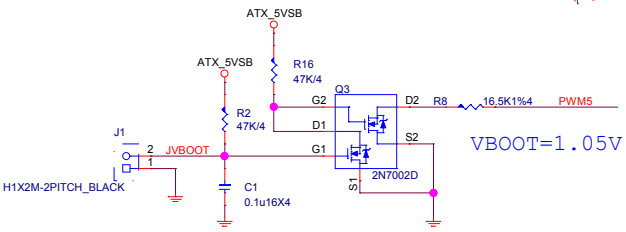
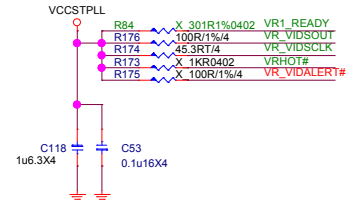
k range : 30%<k<50%

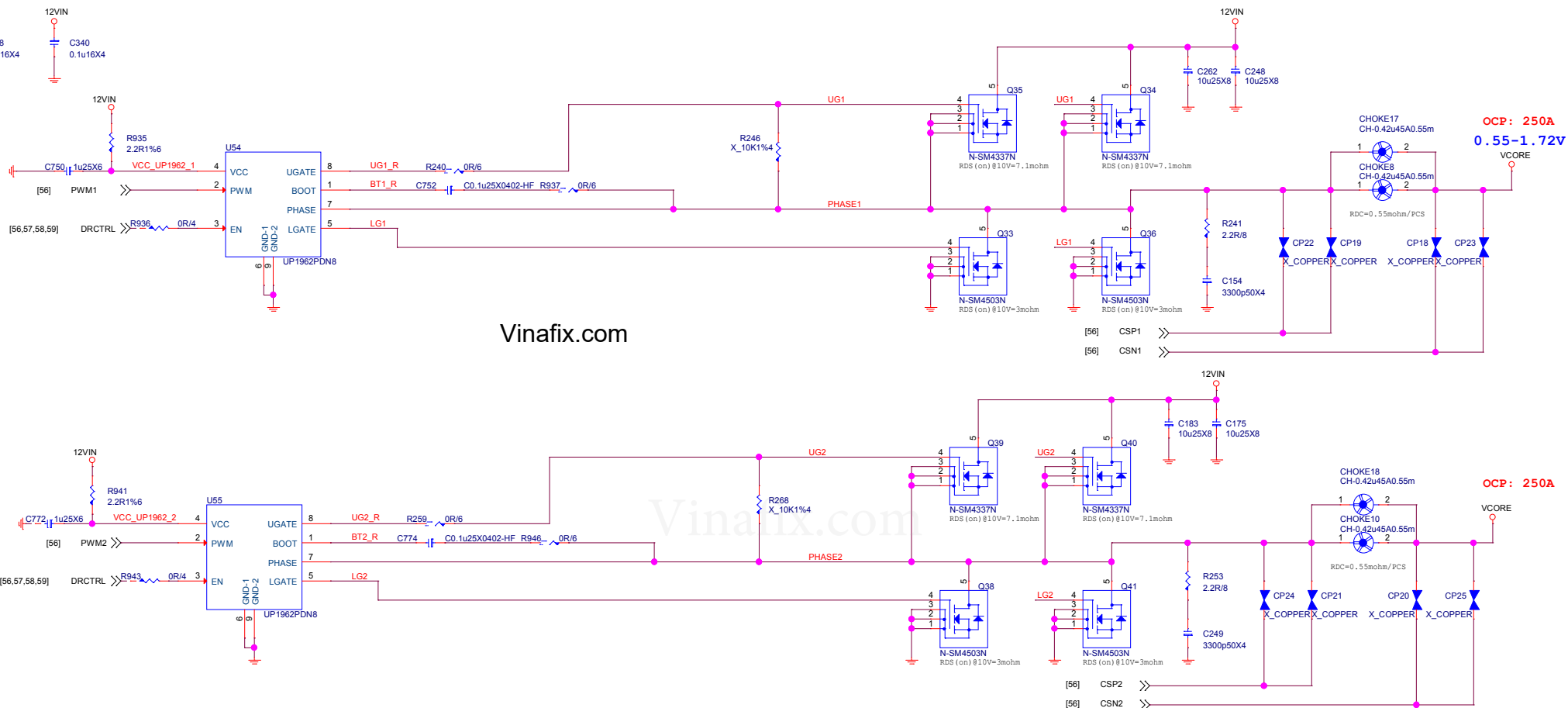


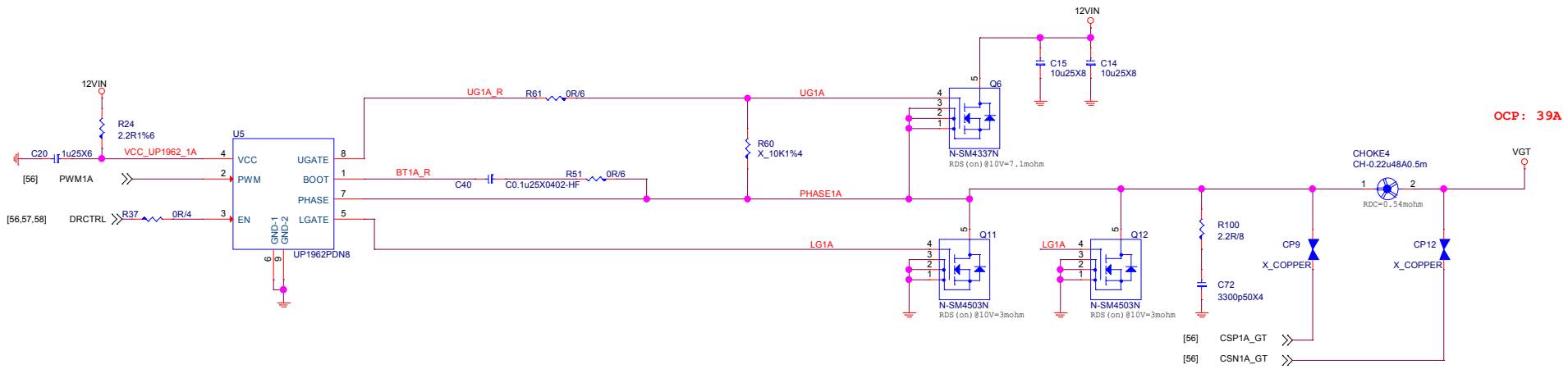


Vcore: ICC Max 193A
LL: 1.6 mohm
OCP: 62.5(Per-Phase)*4Phase=250A

VGT: ICC Max 30A
LL: 3.1 mohm
OCP: 39A(Per-Phase)*1Phase=39A

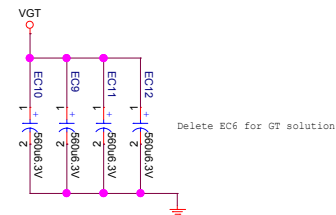






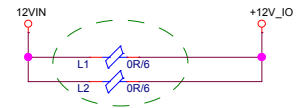
Vinafix.com

Delete VGT 1 Phase 20180425

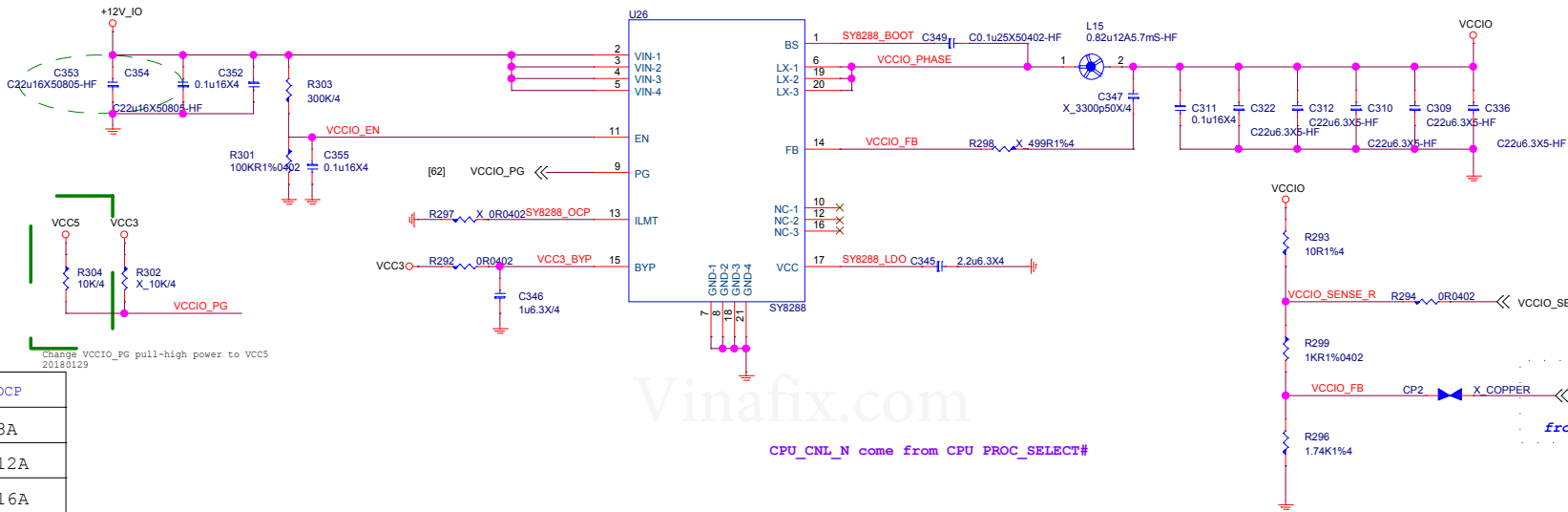


IO Power:0.95V,6.4A

IMAX 10A
ILIMIT=10A~12A
IOC=ILIMIT+40%*IMAX/2=12A~14A.



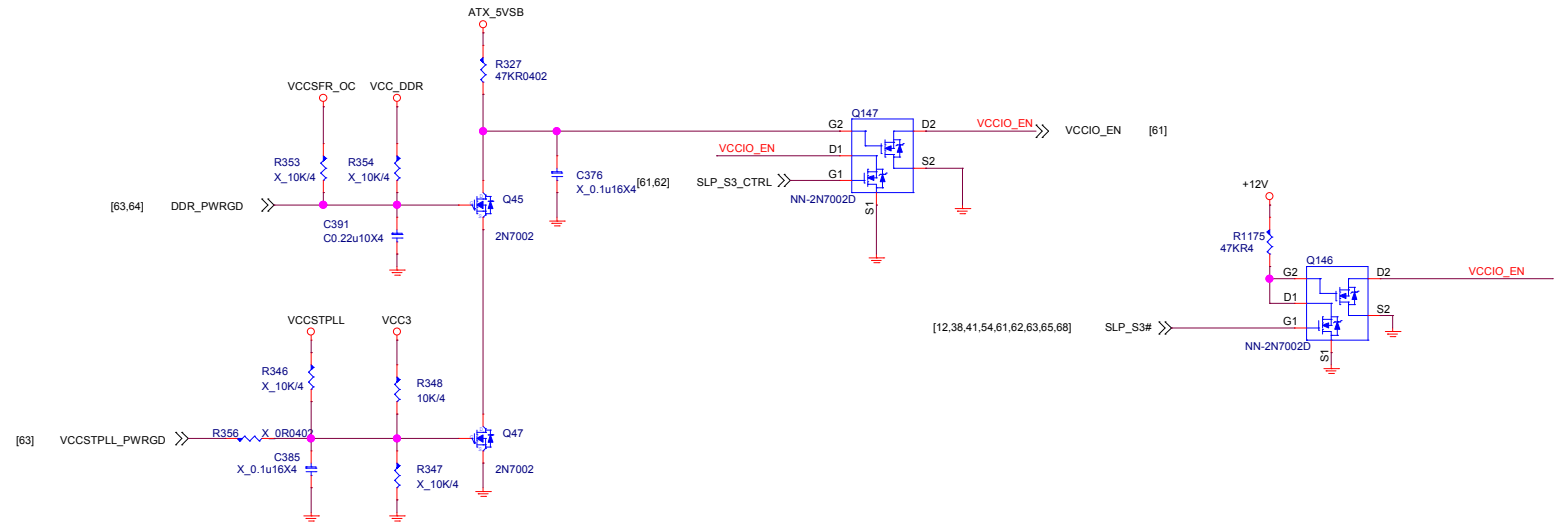
95W
ICCMAX=6.4A
I_{rms} = 1.728A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

Change VCCIO_PG pull-high power to VCC5
20180129

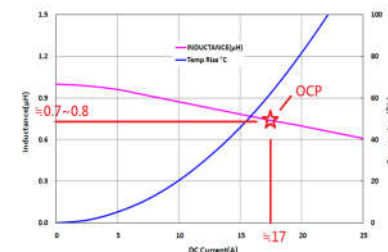
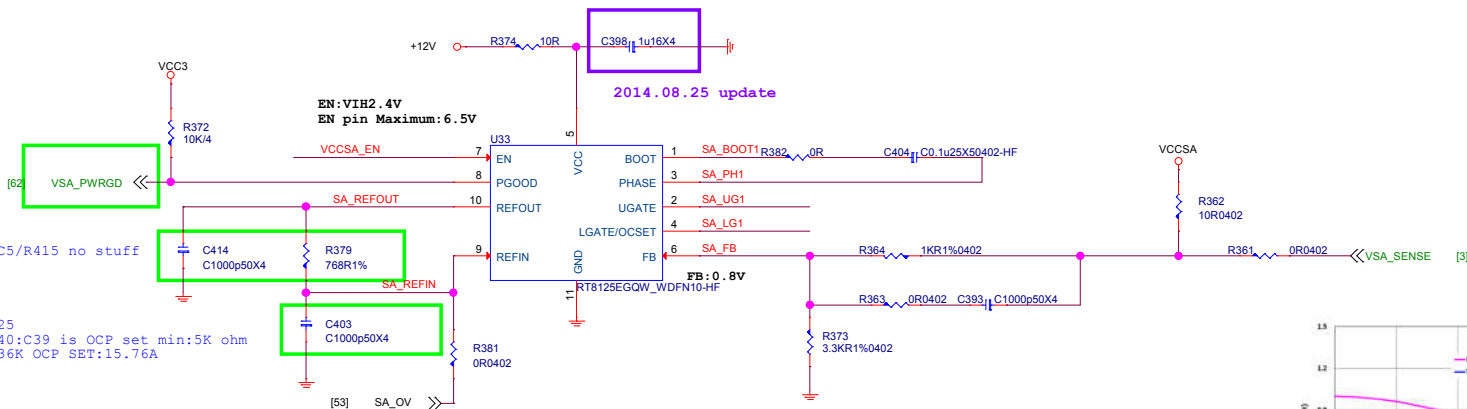
CPU_CNL_N come from CPU_PROC_SELECT#



1.05V; 11.1A

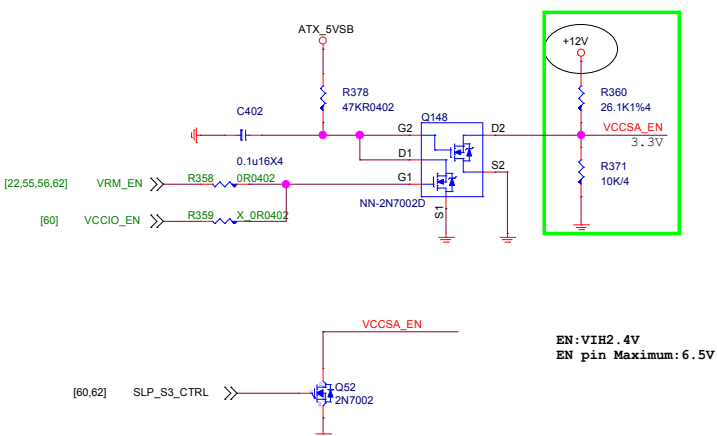
Rdson (low) 10V
D03-4503N0C-ST8 : 3mohm

```
2014.12.25
for up1540:C39 is OCP set min:5K ohm
stuff 5.36K OCP SET:15.76A
```



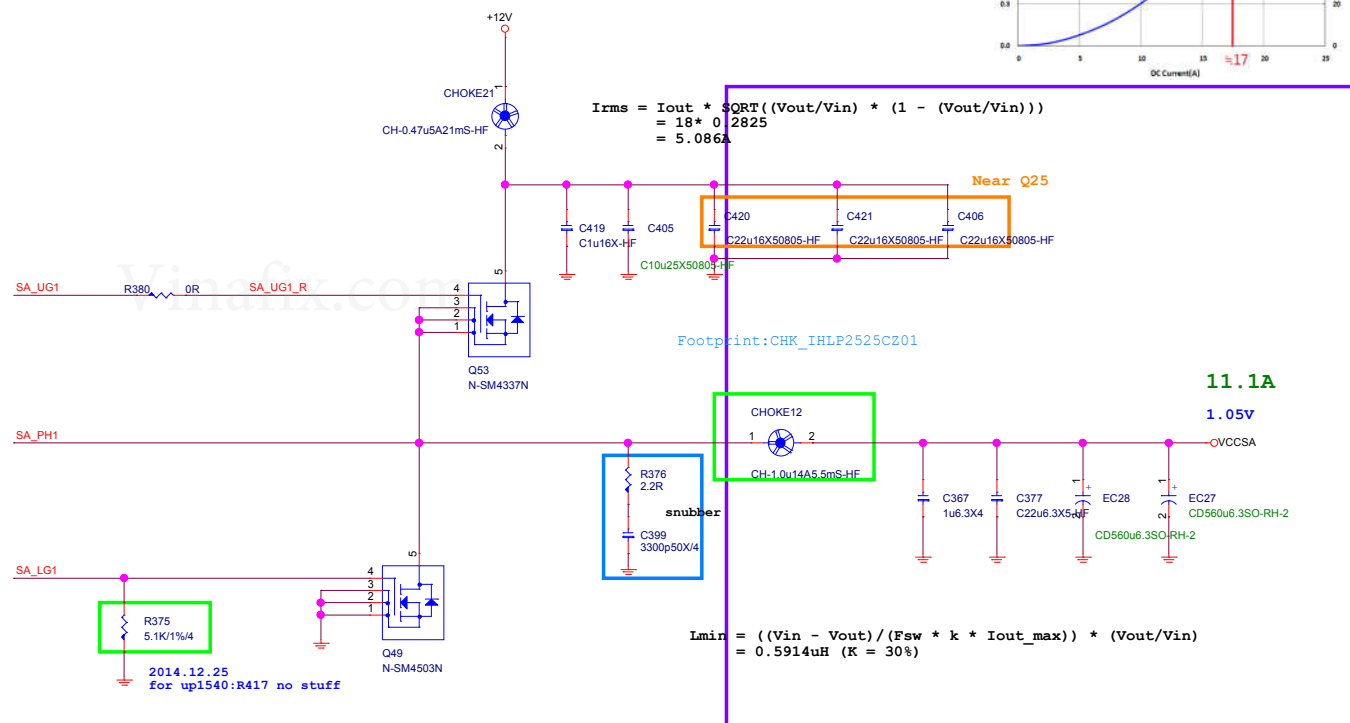
2014.08.21 update

Pull up by layout&Check level



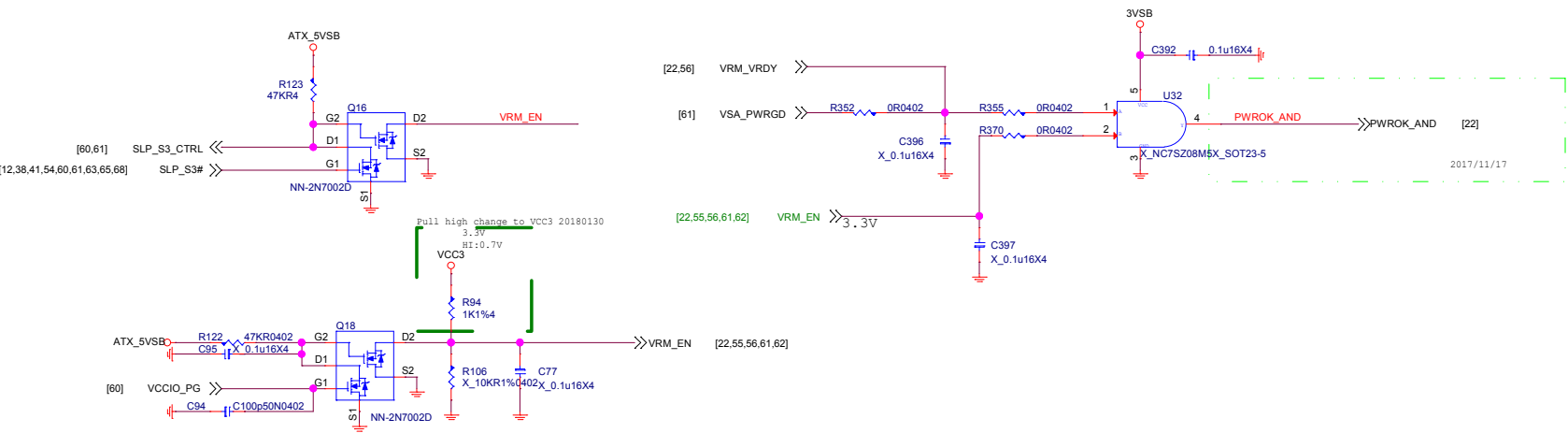
SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

```
SLP_S3# assertion to VR disabled
max:1us
```


$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

$$= 0.5914 \mu H \text{ (K = 30\%)}$$

Sequence



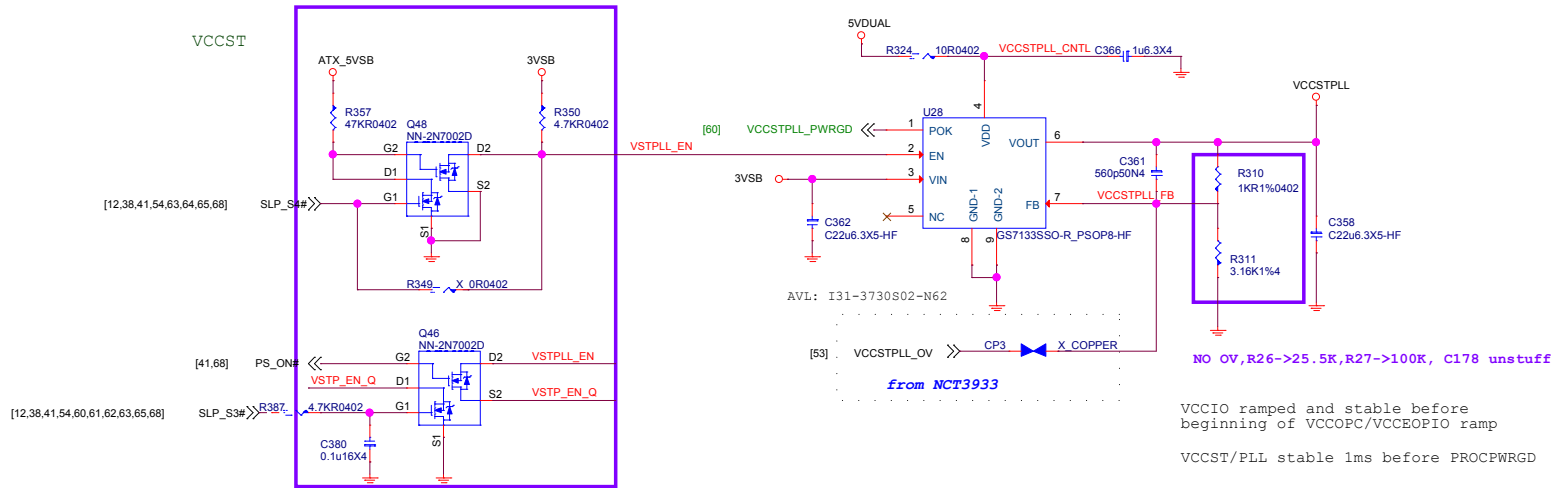
Vinafix.com

VCCSTPLL

1.05V; 230mA

For Cost down VCCST&VCCPLL merge

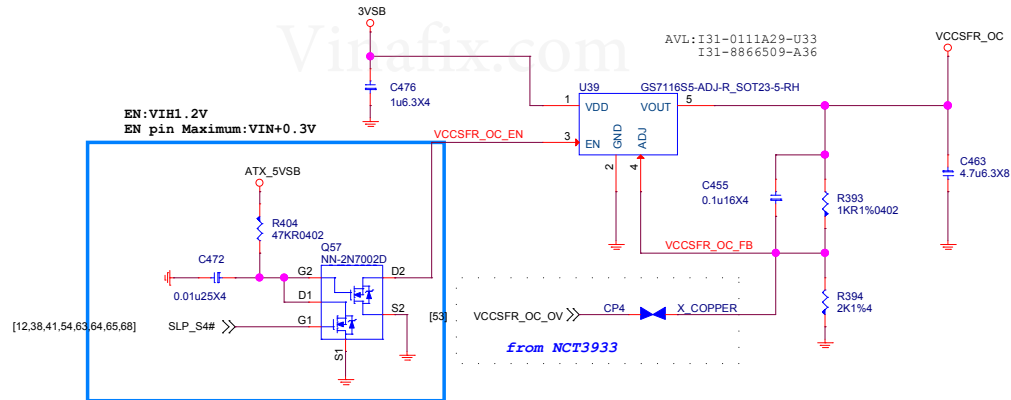
Vinafix.com



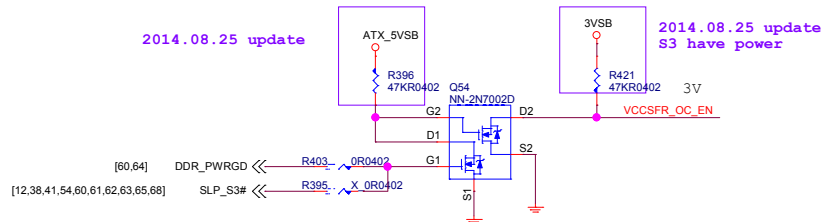
VCCPLL OC

1.2V; 130mA

2014.08.21 update



2014.08.25 update



2014.08.25 update
S3 have power

OCP 27.3

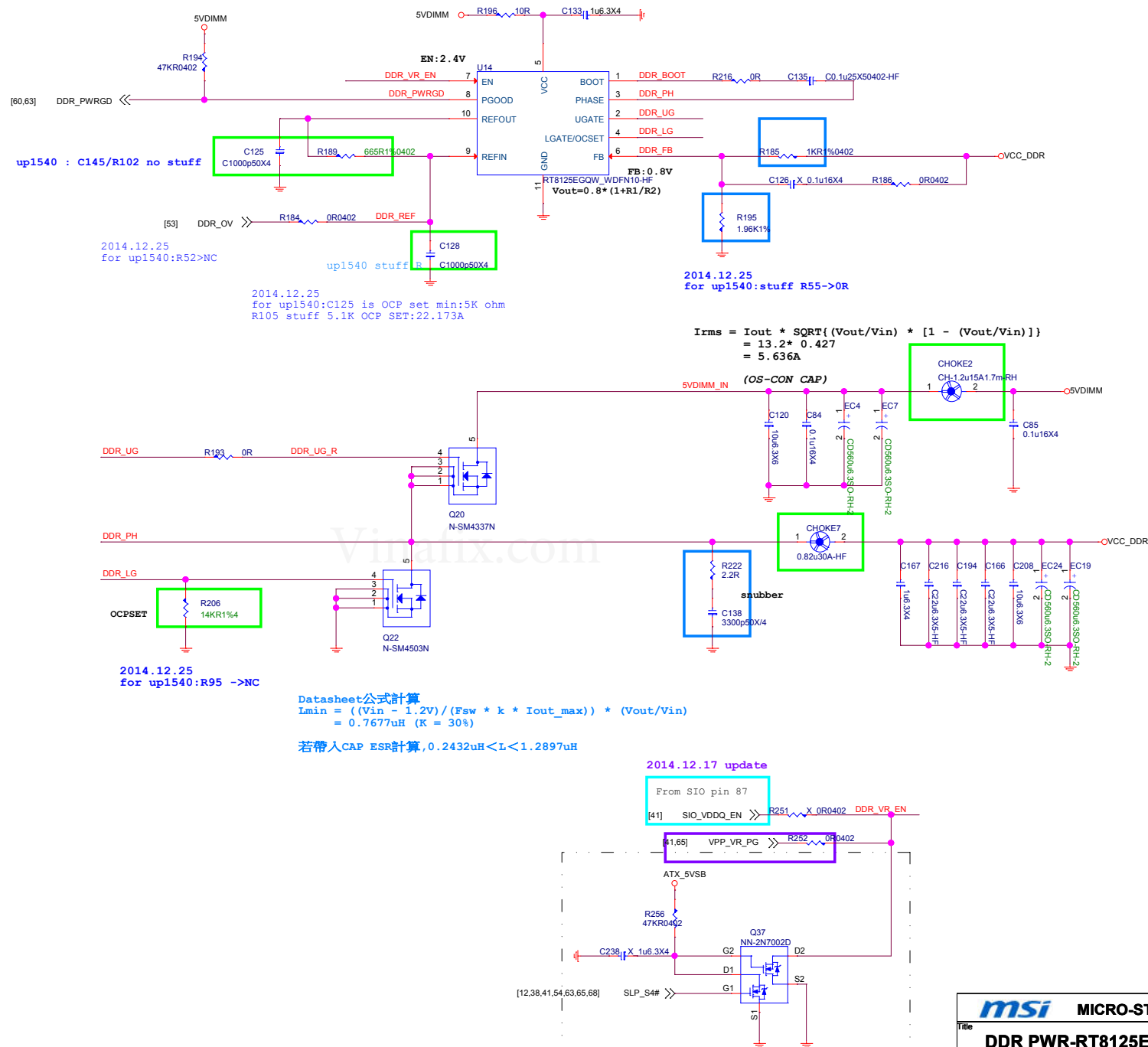
3.3A FOR CPU

15.7A FOR 4DIMM

0.5A FOR DDR
VTT

$$\text{OCP} = 19.5 \times 1.4 = 27.3 \text{ A}$$

$$\begin{aligned} \text{Rocset} &= 1.4 * \text{Imax} * \text{Rdson(LOW)} / \text{Iocset} \\ &= 1.4 * 19.5 * 5.1\text{mohm} / 10\mu\text{A} \\ &= 13.92\text{K} \quad (\text{BOM } \underline{14\text{K}}) \end{aligned}$$

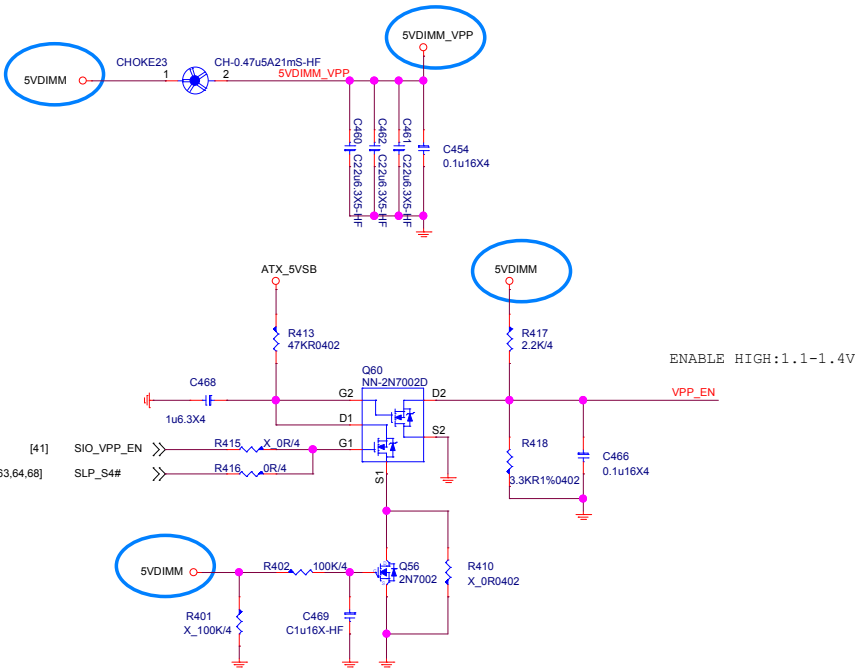


4DIMM :2.24A FOR
DDR VPP2.5V

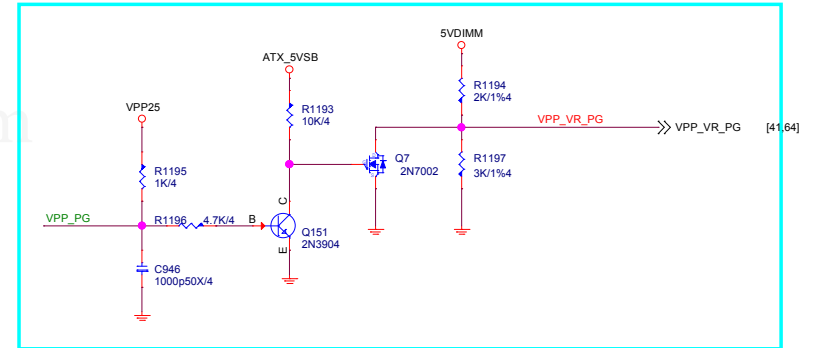
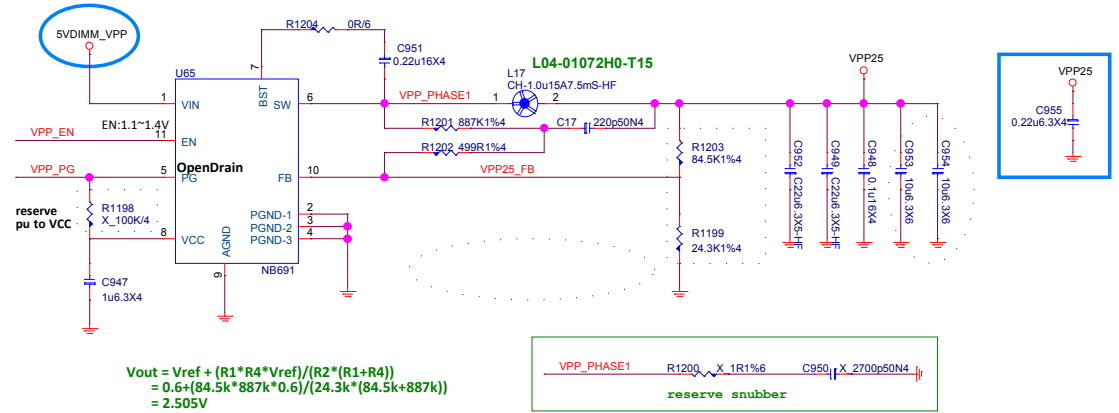
VPP25 Power
2.5V; 2.24A

$$L = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$
$$= 0.9259 \mu H \quad (K = 30\%)$$
$$L = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$
$$= 0.5556 \mu H \quad (K = 50\%)$$

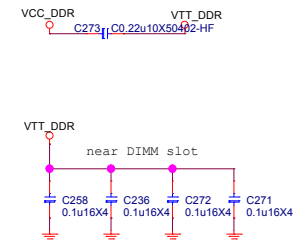
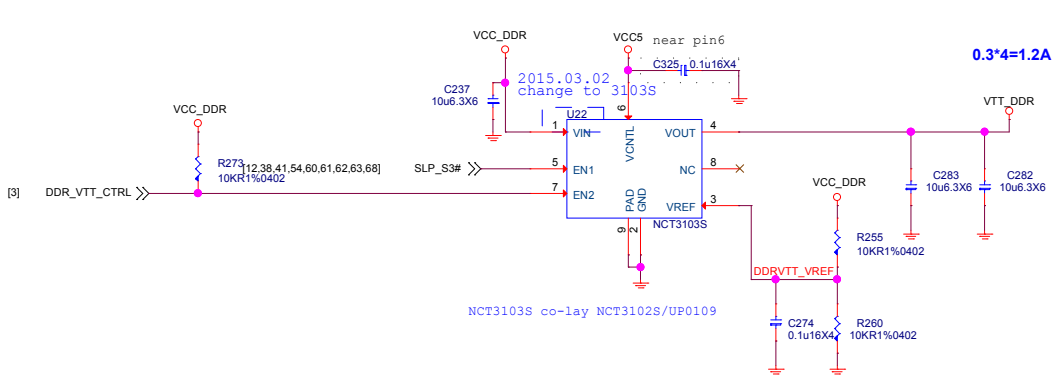
k range : 30%<k<50%



To make sure VPP EN after 5VDIMM stable



DDR VTT Power



1.05V; 13.36A

Rdson (low) 4.5V

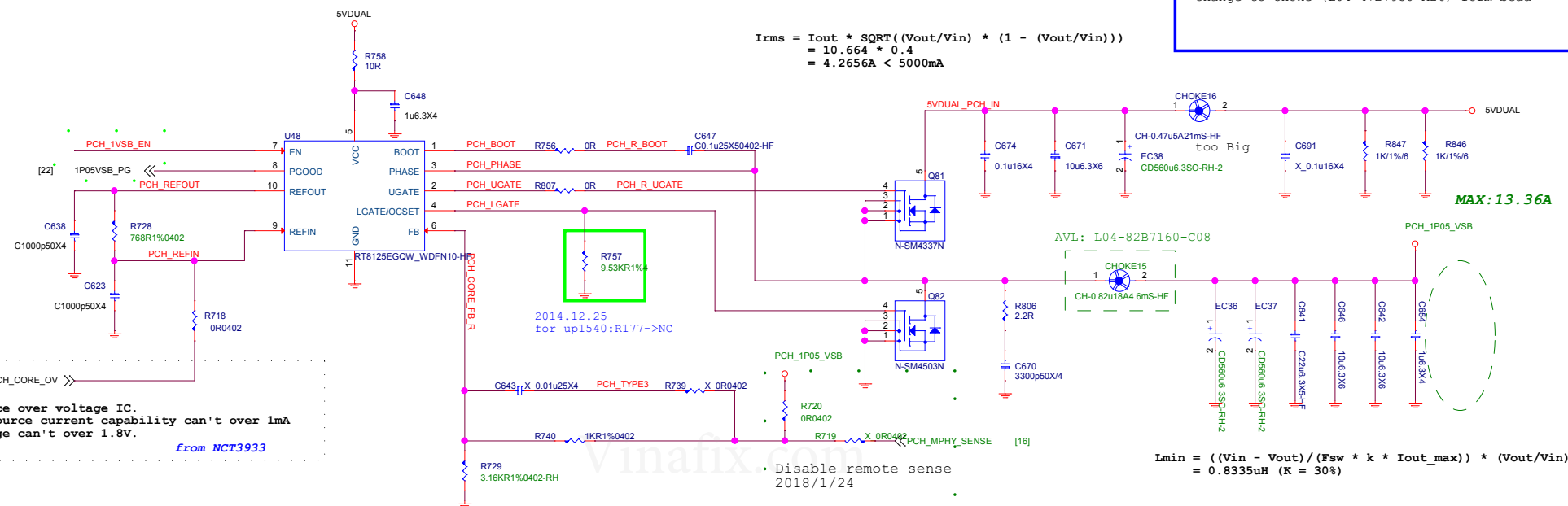
D03-3116M00-U47	:	3.6 mohm
D03-632BA0C-N03	:	4.6mohm
D03-3056M00-U47	:	6.2mohm

$$OCP = 13.36 \times 1.4 = 18.704A$$

```
Rocset = 1.4 * Imax * Rdson(LOW) / Iocset
        = 1.4 * 13.36 * 5.1mohm / 10uA
        = 9.53K
```

Change to Choke (L04-47B7930-M26) form bead

$$\begin{aligned} I_{rms} &= I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))} \\ &= 10.664 * 0.4 \\ &= 4.2656A < 5000mA \end{aligned}$$



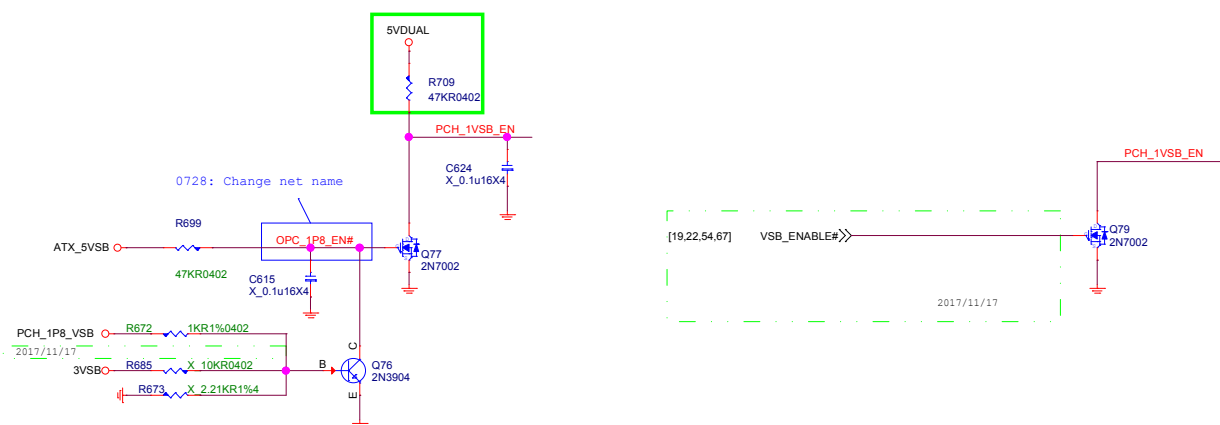
- to sink/source over voltage IC.
- pin10 sink/source current capability can't over 1mA
- So max voltage can't over 1.8V.

from NCT3933

- Disable remote sense

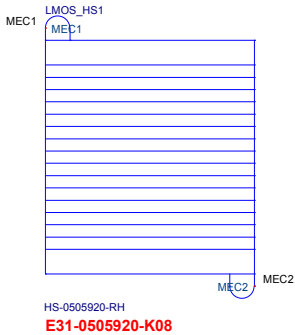
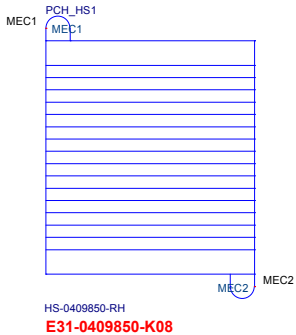
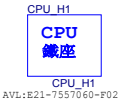
$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out} / V_{in})$$

$$= 0.8335 \mu H \quad (K = 30\%)$$

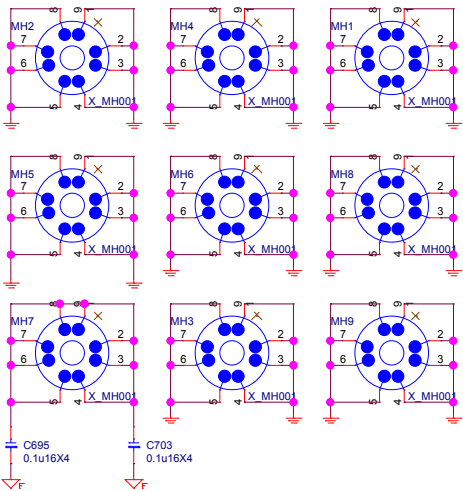




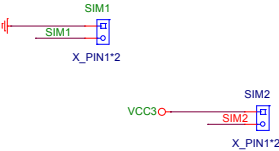
PK0-07B980A-G37, 精成-深圳, 23, 寶安恩斯邁廠 (MSIS)
PK0-07B980A-E48, 競華, 23, 寶安恩斯邁廠 (MSIS)



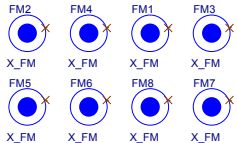
Mounting Holes



Simulation

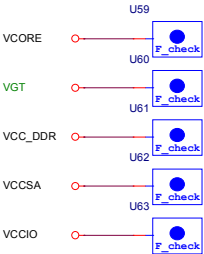


Optical Fiducial Marks-120



Vinafix.com

Vcheck For Factory
Place on BOT



Vcheck

